KAWA ELECTRONIC RESEARCH & DEVELOPMENT CENTRE

Service Manual

Reference No. : SM- LC32AHABCUSXM1-001
Revision : 0
Date : 2006.Jan.25
Page : P.1 of 122

In House Model No. : LCT32HAB
Customer Model No. : LCT3226

BOM No : LC32 .HABCUSXM1 -A01

Description : Service Manual for LCT3226 _CMO_USA

Prepared By: 孫燕

Checked By: **Electronic Engineer** 24/1/06

Mechanical Engineer 24/01/06

Approved By: **Engineering Manager**

Received By: **MK Department**

DOC Rev NO.	The Latest Revision Details	DATE
0	Initial Release	2006-Jan-25

AKAI
SERVICE MANUAL

Model:

LCT3226

Safety Instructions
Production specification.
Block Diagram
Circuit Diagram
Disassembly
Pin Descriptions
LCD Panel specification
Exploded View Diagram
Spare parts list
V-chip password and software upgrade

This manual is the latest at the time of printing, and does not include the modification which may be made after the printing, by the constant improvement of product.

I. Safety Instructions

CAUTION

RISK OF ELECTRIC SHOCK DO NOT OPEN

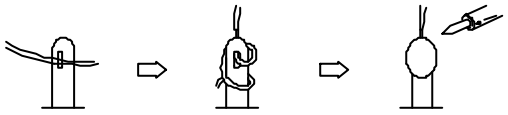
CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated " dangerous voltage" within the product' s enclosure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements. Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulating Tape
   2) PVC tubing
   3) Spacers (insulating barriers)
   4) Insulating sheets for transistors
   5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.

Please leave them at an appropriate depot.

WARNING:

Before servicing this TV receiver, read the X-RAY RADIATION PRECAUTION, SAFETY INSTRUCTION and PRODUCT SAFETY NOTICE.

X-RAY RADIATION PRECAUTION

1. Excessively high can produce potentially hazardous X-RAY RADIATION. To avoid such hazards, the high voltage must not exceed the specified limit. The normal value of the high voltage of this TV receiver is 27 KV at zero bean current (minimum brightness). The high voltage must not exceed 30 KV under any circumstances. Each time when a receiver requires servicing, the high voltage should be checked. The reading of the high voltage is recommended to be recorded as a part of the service record, It is important to use an accurate and reliable high voltage meter.
2. The only source of X-RAY RADIATION in this TV receiver is the picture tube. For continued X-RAY RADIATION protection, the replacement tube must be exactly the same type as specified in the parts list.
3. Some parts in this TV receiver have special safety related characteristics for X-RADIATION protection. For continued safety, the parts replacement should be under taken only after referring the PRODUCT SAFETY NOTICE.

SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this TV receiver. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.

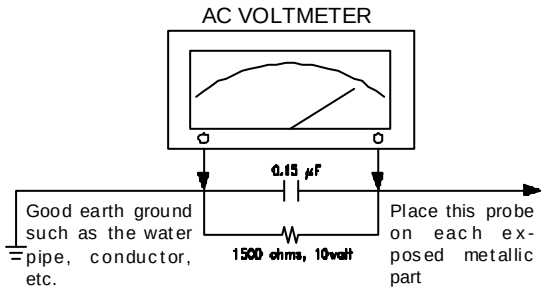
4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.
5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high tempera ture components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads, metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.

   Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15µF AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time.

   Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 uF capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.

   The measured voltage must not exceed 0.3V RMS. This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.

   The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.



AC Leakage Current Check

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this TV receiver have special safety-related characteristics. These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc. The replacement parts which have these special safety characteristics are identified by ⚠ marks on the schematic diagram and on the parts list. Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, X-RAY RADIATION or other hazards.

KAWA ELECTRONIC RESEARCH & DEVELOPMENT CENTRE

Product Specification

Reference No. : **LC32ABHM**
Revision : **0**
Date : **2006.01.23**
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Model No. : **LC32ABHM**
Customer Model No. : **LCT3226**
Design Code : **LC32AB**

BOM No. : **LC32AB**

Artwork Ass'y No. : **580-L32ABHM-TU01L**

Description : **AKAL LCD TV 32" NTSC AC100V-240 V AC USA**

Checked By: **Electronic Engineer** _____

Mechanical Engineer _____

Approved By: **Engineering Manager** _____

Approved By: **PM Department Head** _____

DOC Rev NO.	The Latest Revision Details	DATE
0	Initial Release	

General Description

1. Main features	
Production Description	AKAL LCD TV 32" NTSC AC100V-240VAC USA
Panel Supplier and Model	CHIMEI V320B1-L01
Chips Solution	MK8205
Market	USA
1.1 VIDEO SECTION	
Display size	32"/16:9
Display Resolution	1366 X 768
Pixel Pitch	0.1730mmX 0.5190mm
Peak Brightness	550(nits)
Contract Ratio	1000:1, Typical (1/100 White Window, Dark Room)
View Angle	Hor. And Vert. 170 degree
Color Deeps	16.7M Color (R / G/ B each 256 Scales)
PC Resolution Supporting	VGA, SVGA, XGA,WXGA
HDTV Compatible	480i / 480p / 720p / 1080i
Progressive Scanning	Yes
Film Mode Pull Down	Yes
"GAMMA" Correction	Yes
Color Temperature Control	Yes
Comb Filter	Yes
Second De-interlace for Sub picture	No
Wide Mode	Full,Fill Aspect Ratio,Nonliner,LB to 16:9, LB subtitles to 16:9 or Anamorphic
TV System	NTSC M
Dual Tuner System	No
AV Input Color System	PAL /NTSC
PIP	Basic mode (video on graphic mode,resolution 1024×768)
1.2 AUDIO SECTION	
Audio Output Power	10W×2 Max.(8 ohm)
Sound Effect	NO
Tone Control	Yes
1.3 Input Terminals	D-Sub 15 Pin Type(Analog-RGB Input) ×1 DVI-D with HDCP (29 Pin) ×1 Component Video-YPbPr/YCbCr ×2 RCA Terminals S-Video Input (Mini Din 4Pin) ×1 Video Input RCA Terminals Y / Pb / Pr, Y / Cb / Cr (RCA Type) ×2 Stereo Audio Input for YPbPr / YCbCr x 2 (3.5mm Phone Type) ×1
1.4 Output Terminals	Audio Output (RCA ; L&R Type) ×1
1.5 Others	
Closed Caption / V-Chip	Yes
Teletext No	
OSD Language	English, Français, Español

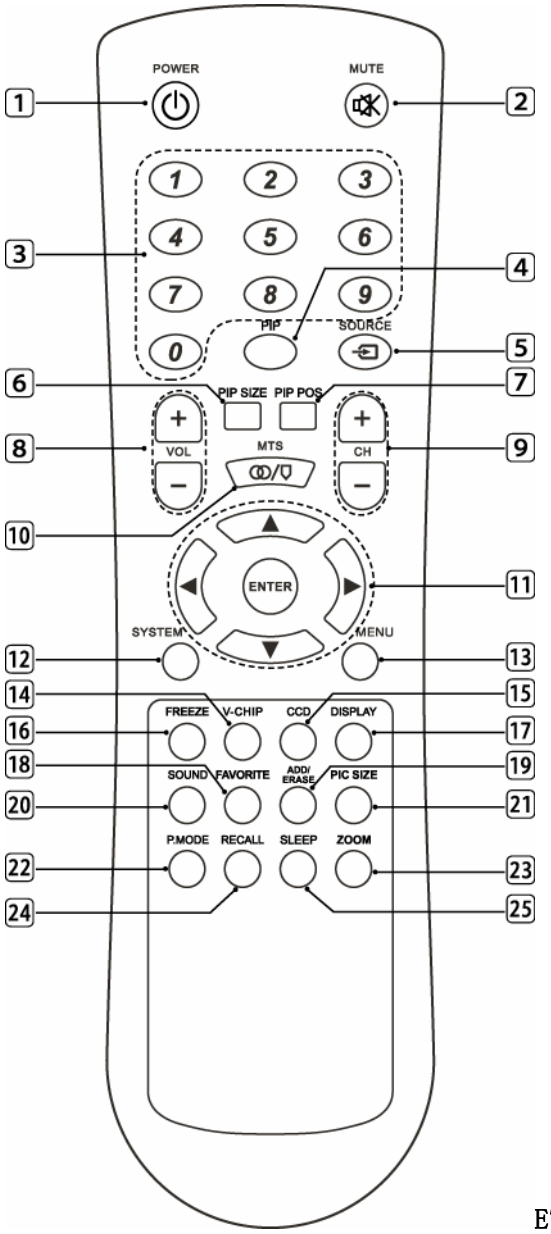
Stereo Decode	**MTS with SAP**
Power Rating	**AC 100-240V, 50/60Hz**
Power Consumption	**200W**

1.6 Support the Signal Mode
This machine can support the different from VGA signal mode in 11 kinds

No	Resolution	Horizontal Frequency(Hz)	Vertical Frequency(KHz)	Dot Clock Frequency(MHz)
1)	640×480	31.50	60.00	25.18
2)	640×480	37.86	72.81	31.50
3)	800×600	35.16	56.25	36.00
4)	800×600	37.90	60.32	40.00
5)	800×600	46.90	75.00	49.50
6)	800×600	48.08	72.19	50.00
7)	1024×768	48.40	60.00	65.00
8)	1024×768	56.50	70.00	75.00
9)	1024×768	60.00	75.00	78.75
10)	1280×720	45.00	60.00	108.04
11)	1280×1024	64.00	60.01	108.00

1.7 HDTV Mode (YPbPr)

No	Resolution	Horizontal Frequency(KHz)	Vertical Frequency(Hz)	Dot Clock Frequency(MHz)
1)	480i	15.734	59.94	13.50
2)	480p(720×480)	31.468	59.94	27.00
3)	720p(1280×720)	45.00	60.00	74.25
4)	1080i(1920×1080)	33.75	60.00	74.25

2. LCD local control button	**Main power : push switch** **Channel +/- volume up/down menu input. standby : soft touch**
3. Led indicators :	**Power on: Green** **Standby: Red**
4. OSD language	**English, Français, Español**
5. OSD	**Full on screen display**
6. Remote control unit **Customer Remote** **Code: 609F(NEC)** **1 POWER button** **2 MUTE button** **3 0-9 DIGITAL button** **4 PIP button** **5 SOURCE button** **6 PIP SIZE button** **7 PIP POS button** **8 VOL +/- button** **9 CH +/- button** **10 MTS button** **11 UP/DOWN,LEFT/RIGHT ENTER buttons** **12 SYSTEM button** **13 MENU button** **14 V-CHIP button** **15 CCD button** **16 FREEZE button** **17 DISPLAY buttons** **18 FAVORITE button** **19 ADD/ERASE buttons** **20 SOUND button** **21 PIC SIZE button** **22 P.MODE button** **23 ZOOM button** **24 RECALL button** **25 SLEEP button**	 E7501-051001
7. Safety standard	**UL/FCC/cUL**
8. EMC standard	**15 Parts of the FCC rules,CLASS B**
9. Performance standard	**LCD-TV Standard**
10. Accessories	**Battery 2pcs** **User Manual 1pcs** **AC Cable 1pcs** **Remote Control 1pcs** **The Accessories box 1pcs**

Technical Data

1. Chassis		MICO
2. Power supply	TV	AC 100-240 V, 50/60Hz
	Remote controller	Battery 3V (UM-4/R03/AAA×2)
3. TV system	RF input	NTSC M
	Video input	PAL/NTSC 3.58/NTSC 4.43
4. Receiving channels	TV	VHF-L : 2~6CH VHF-H : 7~13CH UHF : 14~69CH
	CATV	1~125CH
5. Intermediate frequencies	Picture	45.75MHz
6. Scanning	Horizontal (Hz)	15625/15750
	Vertical (Hz)	50/60
7. AC plug		UL Plug
8. Panel		V320B1-L01
9. Speaker	Internal	8 ohm 10W (max) ×2
10.Operating temperature	Fulfill all specifications	15 C ~ 30 C
	Accept picture/sound reproduction	5 C ~ 33 C
11. Operating relative humidity	Fulfill all specifications	45% ~ 75%
	Accept picture/sound reproduction	20% ~ 80%
12. Electrical & optical specification		See the attachment 1.
13. Circuit diagram drawing No.		LC32ABHM
15. Cabinet		
16. Cabinet color		
17. Packing		1 set per
18. Container stuffing method		RD/05/P/LC32HAB/CSI/02 REV: 01
19. Dimension (mm) (No packing)	LCD-TV	988(W) x 514(H) x 94(D)mm (w/o Stand)
		988(W) x 582(H) x 268(D)mm (with Stand)
	Remote control unit	183(L) x 53(W) x 28(T)mm
20. Net weight	LCD-TV	15.5Kg (with Stand) approx.
	Remote controller	70g (approx.)
21. Cell Defect		Subject to Panel supplier specification

Attachment 1： Electrical & Optical Specification

No.	*Items*	*Instruction*	*Typical*	*Limit*	*Unit*
1	Video sensitivity	For 30dB S/N	44	≤51	dBuV
2	FM sound sensitivity	For 30dB S/N	21	≤35	dBuV
3	Color sensitivity	For RF transmission	37	≤40	dBuV
4	CCD sensitivity	TV screen refreshes 40 times number of mistakes≤8	43	≤50	dBuV
5	Minimum NICAM threshold	Without crackline noise	N/A	N/A	dBuV
6	Stereo Channel Separation	BTSC.	18	≥15	dB
7	AGC static characteristic	Accept. Picture/Sound repr.	90	≥90	dBuV
8	Selectivity	Adjacent sound carrier	30	≥28	dB
		Below adjacent sound carrier	30	≥30	
		Adjacent picture carrier	45	≥40	
		Up adjacent picture carrier	40	≥30	
9	IF rejection		55	≥45	dB
10	Image rejection	VHF	57	≥45	dB
		UHF	55	≥40	
11	AFT pull-in range		±1.0	≥|±1.0|	MHz
12	Chroma sync pull-in range		±500	≥|±200|	Hz
13	Color killer function		-11	≤-10	dB
14	Resolution — RF — Horizontal	PAL	300	≥300	Lines
		NTSC	260	≥240	Lines
	RF — Vertical	PAL	410	≥400	Lines
		NTSC	320	≥300	Lines
	Video — Horizontal		450	≥450	Lines
	Video — Vertical		400	≥400	Lines

15	Color Coordination	White	Xw	Full Pattern	0.295	0.295±0.02	
			Yw		0.300	0.300±0.02	
16	View Angle(Lo/3)	Horizontal			170	≥170	Degree
		Vertical					
17	Overscan			Cross hatch signal	96	94~98	%
18	Picture position			In all direction	±2	≤|±3|	mm
19	H sync pull-in range				±400	≥|±200|	Hz
20	V sync pull-in range				6	≥6	Hz
21	Audio frequency response			±3dB ref. to 1KHz	0.15~12	0.2~12	KHz

22	Max Audio Output Power		7×2	≥5.0×2	W
23	Audio output power 10% THD	1KHz 10% THD	6×2	≥4.0×2	W
24	THD	Po=0.5W	0.5	≤3	%
25	Signal to buzz ratio	coeighting	50	≥30	dB
26	Minimum volume hum	coeighting	6	≤10	mVrms
27	Maximum woofer output power		N/A	N/A	W
28	Woofer audio frequency response	±3dB ref. to 15Hz AV mode	N/A	N/A	Hz
29	Tone low frequency	100Hz ref. to 1KHz AV mode	±8	≥|±3|	dB
30	Tone high frequency	10KHz ref. to 1KHz AV mode	±8	≥|±3|	dB
31	Balance	Center	0	≤|±2|	dB
		Max.	3	>2	
		Min.	-35	≤-30	

32	Video input level		1.0	1±0.3	Vpp
33	Audio input level*（1）		1.0 *	0.5±0.3	Vrms
34	Video output level		N/A	N/A	Vrms
35	Audio output level*（2）		0.3 *	0.5±0.3	Vrms
36	AV Audio input max. level		2	≤2	Vrms
37	AV Audio output L/R Separation		35	≥30	dB
38	Power consumption	Operating	200	≤200	W
		Stand by	3	≤5	W
39	IR receiving distance	0 Degree	7	≥6	m
40	IR receiving angle left/right	5m	60	≥45	Degree
	IR receiving angle Up/down		20	≥15	Degree
41	Dielectric strength	DC 3KV 1min.	5	≤10	mArms
42	The vibration noise from electromagnetic devices in LCD-TV set	The distance between the tester and the LCD-TV set is four times as many as the screen height	No obvious vibration noise can be heard		

Test Condition

All tests shall be performed under the following conditions unless otherwise specified

1	**Picture Modulation**	**87.5%**
2	**Sound Modulation**	**27KHz Dev. For DK/I/BG** **15KHz Dev. For M/N**
3	**Picture to Sound Ratio**	**10dB**
4	**Sound Artificial Load Resistor**	**8 ohm**
5	**Video signal**	**Stair and Special**
6	**Audio signal**	**1KHz sine wave 0.5Vrms**
7	**Other conditions:** **A. Switch LCD-TV on and let it warm up for more than 30 minutes.** **Viewing distance: 3H (H: Panel High) in front of LCD, about 2M.** **Ambient light: ≤0.1 cd/ m^2** **B. Brightness, Contrast, Saturation, Tint, sharpness set at normal.** **C. Connect RMS volt meter to speaker terminals and adjust the LCD volume to get 500mW RMS power at each terminals.** **D. With image sticking protection of LCD module. The luminance will descend by time on a same still screen and rapidly go down in 5 minutes, when measuring the color tracking and luminance of a same still screen, be sure to accomplish the measurement in one minute to ensure its accuracy.** **E. Due to the structure of LCD module. The extra-high-bright same screen should not hold over 5 minutes for fear of branding on the panel.** **F. RF test point: Video output.**	
8	**Note:** ***(1) Now this project cannot fit the limited spec. the typical audio input level is 1.0 Vrms,** ***(2) The audio out level is controlled by the volume level, the range is from 0 to 0.5Vrms.**	

1.Do not power on .

1.1 Please check AC cable if connect to AC plug.

Is true the connector don’t connect to AC plug. Please connect it.

2.2 Please check AC cable if connect to AC power.

Is true the AC cable don’t connect to AC power. Please connect it.

3.3 Please check power board of fuse if broken.

If the F1 fuse is broken, Please pull out the AC cable from AC power. Please check AC L power and AC N ground by multimeter, The read number is infinite, the fuse is broke. then look up power board if not burn out place. Is true it. Please change power board or be changed power board.

2. The power on switch of green extinguish.

2.1 The power of led(indicator light) is red light, To touch power on key when indicator light wink.

Is true that the power DC output have somewhere short circuit.

Please check connector J1,J21 and TV board J3,J1. If not connector direction is wrong.

Or the connect wire is direction is wrong.

3.The power is normal work ,but don’t backlight.

3.1 The indicator light work normal (green light).

Please check Main board of transistor Q6 collect if not has +5v voltage.

Is true Q6 collect hasn’t +5v ,To check Q6 if fail.

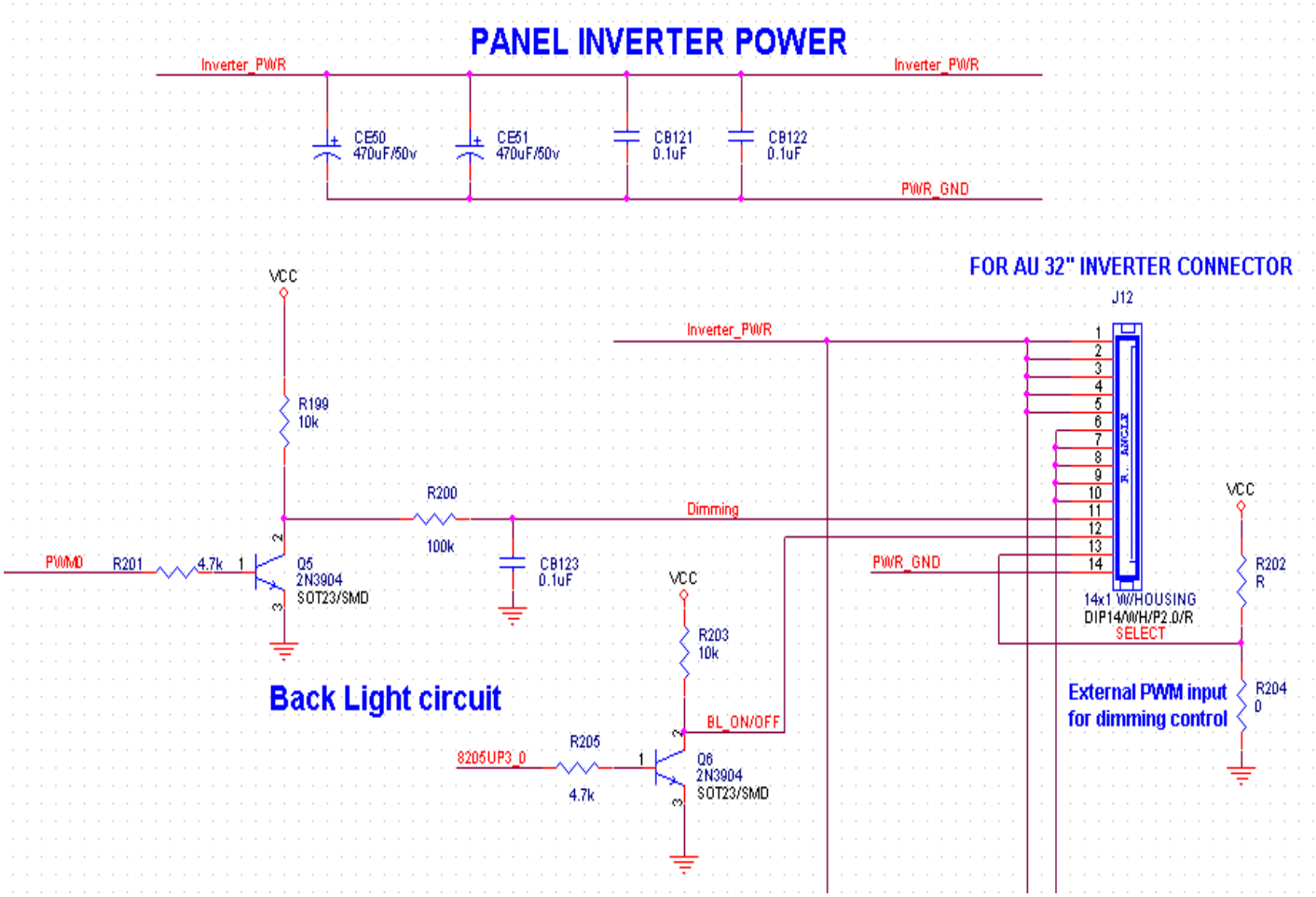
3.2 Please check backlight of connector if not it direction is wrong or the connector of wire compositor direction is wrong.

..The panel backlight(inverter) connector of wire compositor direction follow down:

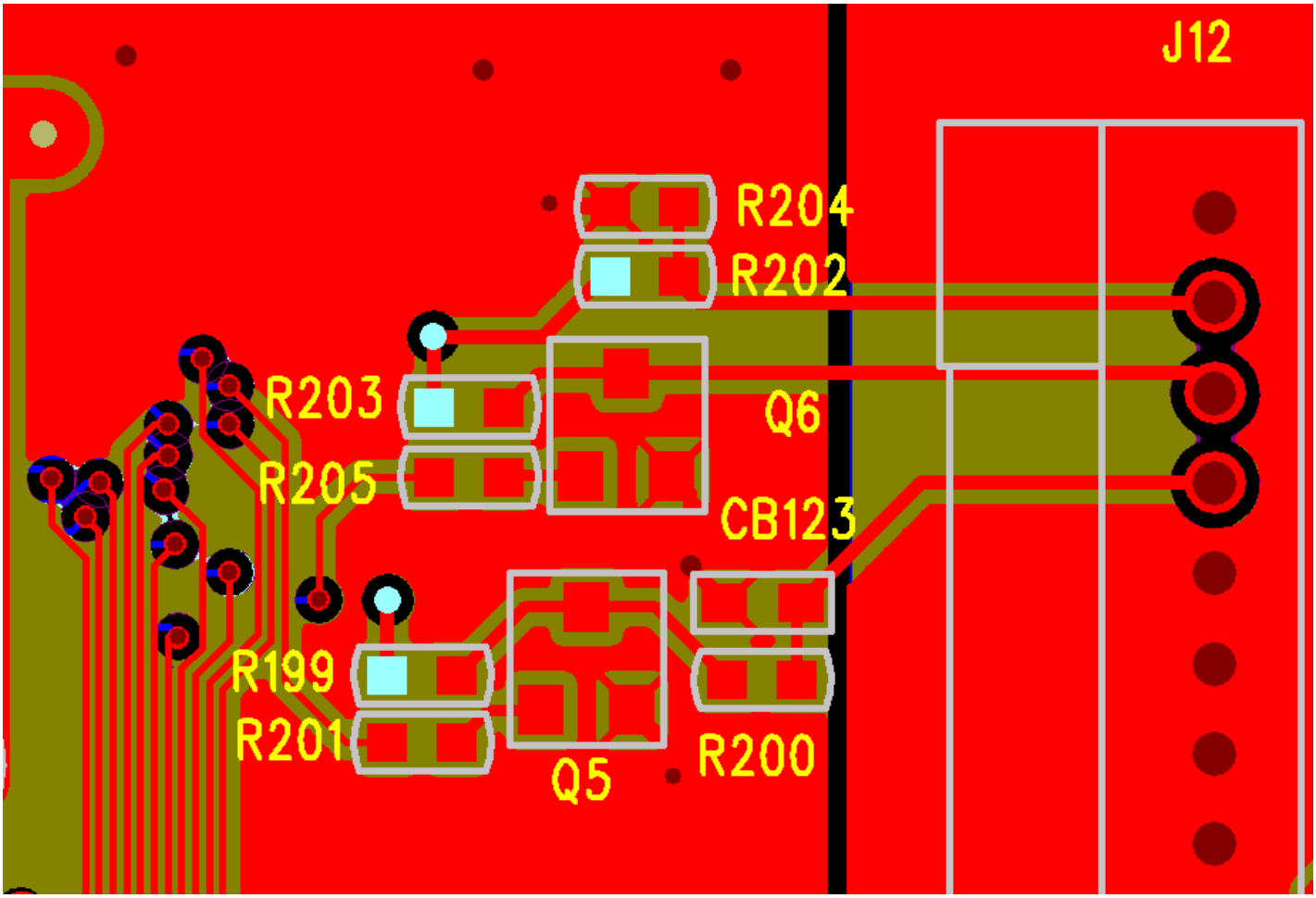
Pin No.	Symbol	Description
1	VBL	+24V Power input
2		
3		
4		
5	NC	NC
6	GND	Ground
7		
8		
9	SEL	Internal/external PWM selection High : external dimming Low : internal dimming
10	E_PWM	External PWM control signal E_PWM should be connected to low when internal PWM was selected (SEL = low).
11	I_PWM	Internal PWM control signal I_PWM should be connected to ground when external PWM was selected (SEL = high).
12	BLON	Backlight on/off control

.

.To control Backlight circuit diagram follow down:



PCB photo follow down:

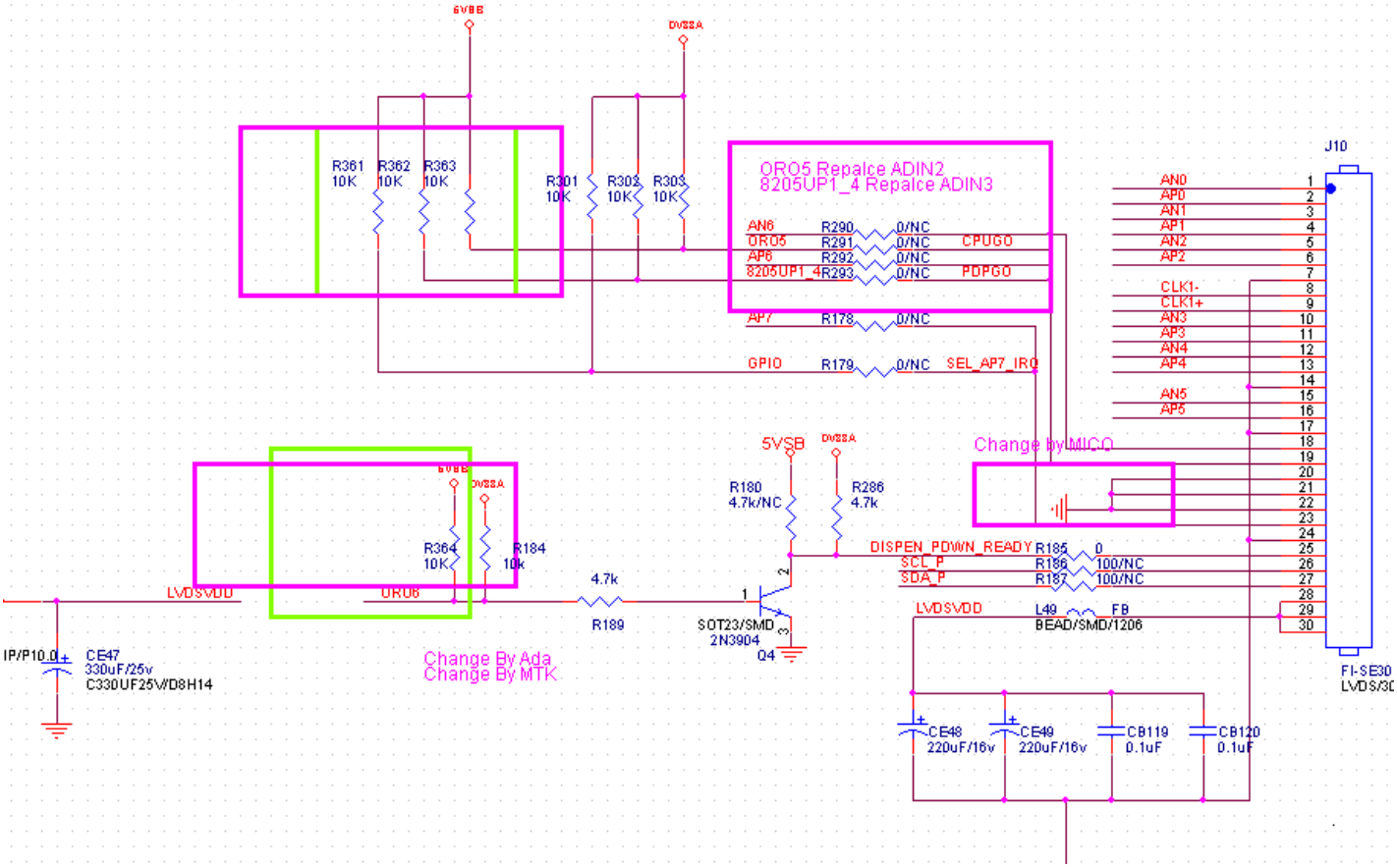


To check connector J12 of the first pin if it have +5V voltage. It’s true , than to check power board of +24v voltage ,It’s true. The panel of backlight board is fail. The change panel of backlight board.

4.The screen don’t have picture But have backlight.

4.1 To check to panel of voltage ,To check main board of J10 of the twenty eighth ,ninth and thirtieth . It’s true +5v voltage.

Circuit diagram follow down:

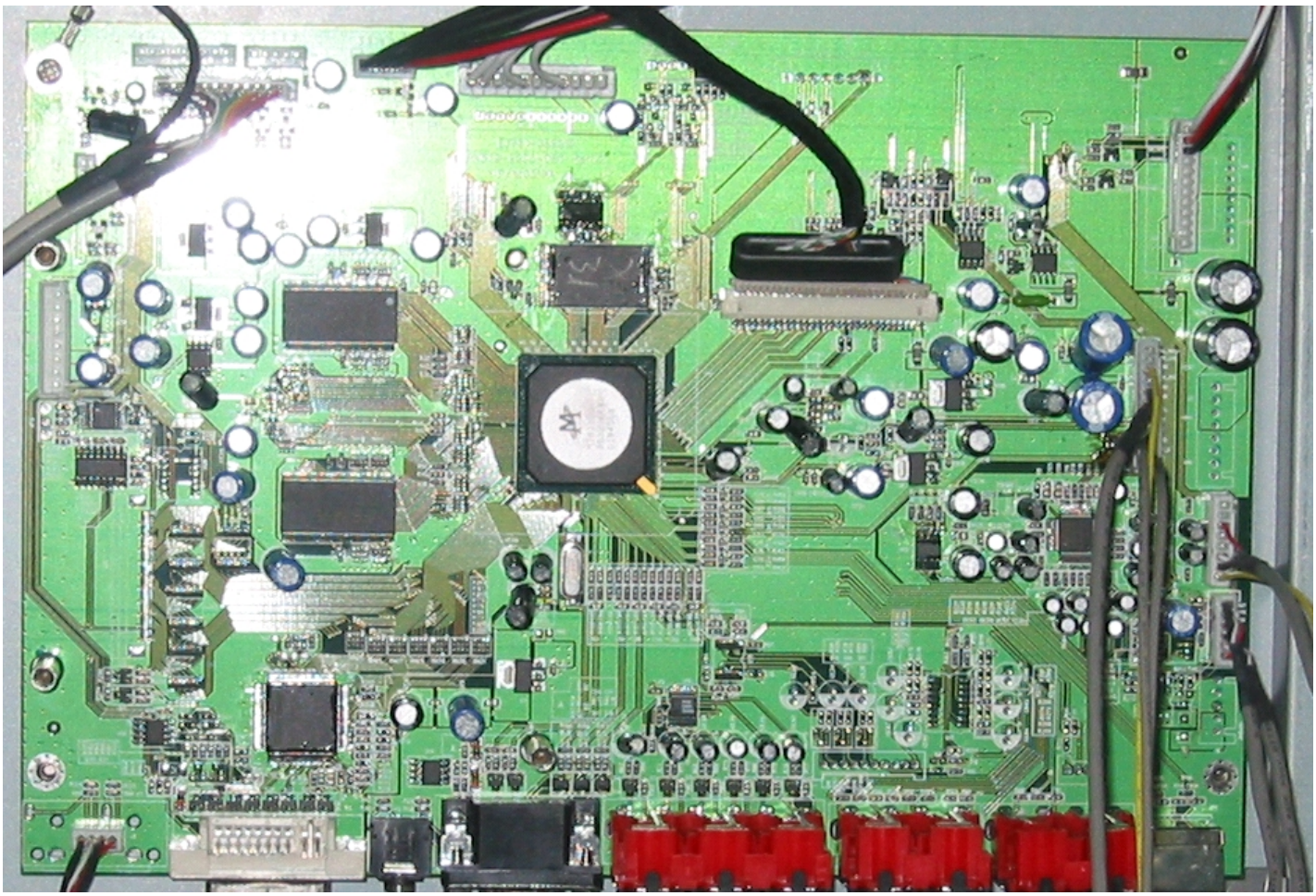


The panel of connector define diagram follow down:

CNF1 Connector Pin Assignment

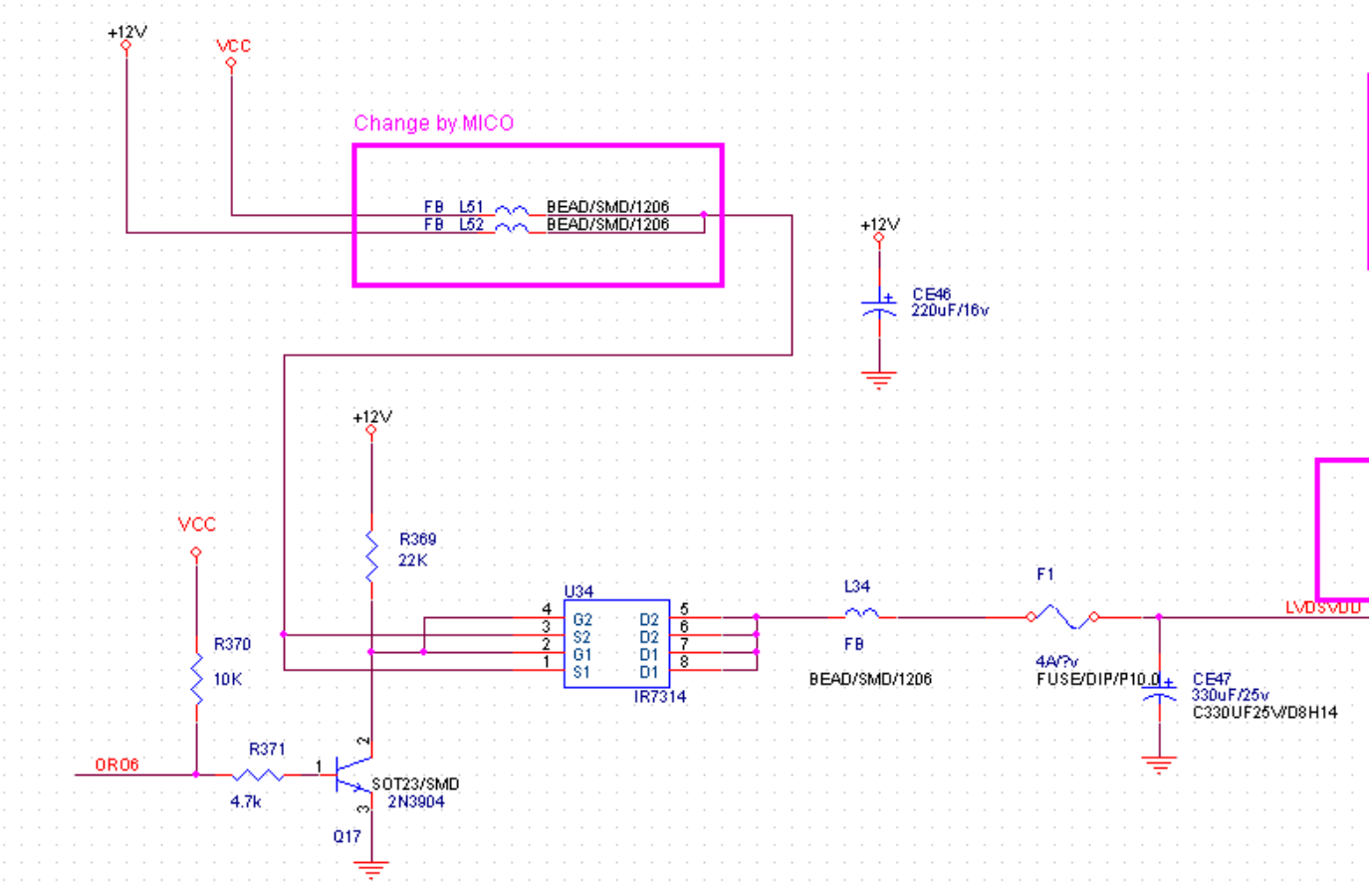
Pin No.	Symbol	Description	Note
1	GND	Ground	
2	RPF	Display Rotation	(3)
3	SELLVDS	Select LVDS data format	(5)
4	NC	No Connection	(2)
5	NC	No Connection	
6	ODSEL1	Overdrive Lookup Table Selection	(4)
7	ODSEL2	Overdrive Lookup Table Selection	
8	GND	Ground	
9	RX0-	Negative transmission data of pixel 0	
10	RX0+	Positive transmission data of pixel 0	
11	RX1-	Negative transmission data of pixel 1	
12	RX1+	Positive transmission data of pixel 1	
13	RX2-	Negative transmission data of pixel 2	
14	RX2+	Positive transmission data of pixel 2	
15	RXCLK-	Negative of clock	
16	RXCLK+	Positive of clock	
17	RX3-	Negative transmission data of pixel 3	
18	RX3+	Positive transmission data of pixel 3	
19	GND	Ground	
20	GND	Ground	
21	GND	Ground	
22	GND	Ground	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	
26	VCC	Power supply: +5V	
27	VCC	Power supply: +5V	
28	VCC	Power supply: +5V	
29	VCC	Power supply: +5V	
30	VCC	Power supply: +5V	

Main board connect wire photo follow down:

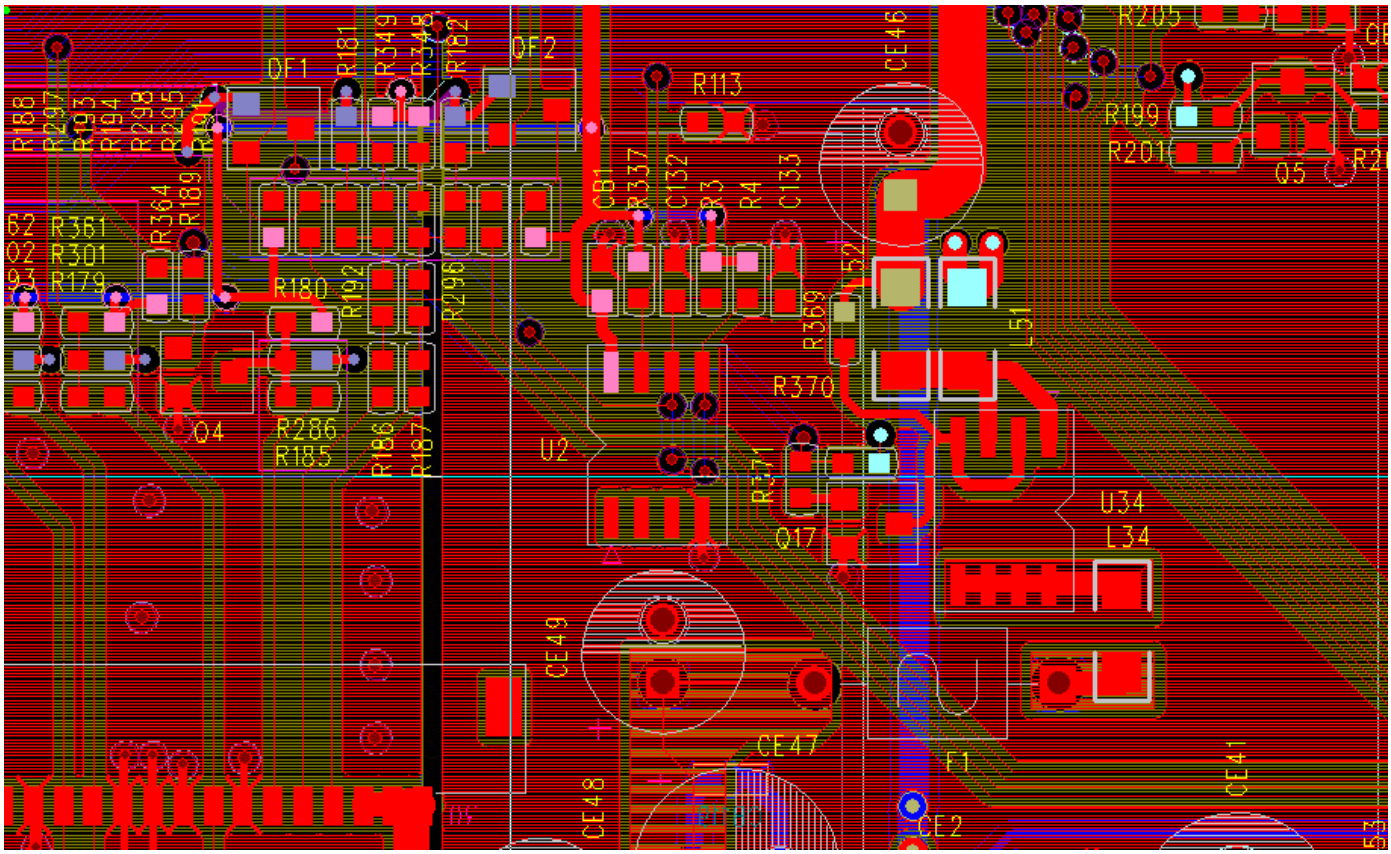


4.2To check to main board +5v voltage. To check to main board IC U34 of the first pin if +5v voltage or check FB L51. It’s true +5V voltage, then check main board of F1 if +5v voltage .If not. Again to check Q17 of base is high level or low level .if high level is OK. Is low level is fail.

The circuit diagram follow down:



PCB

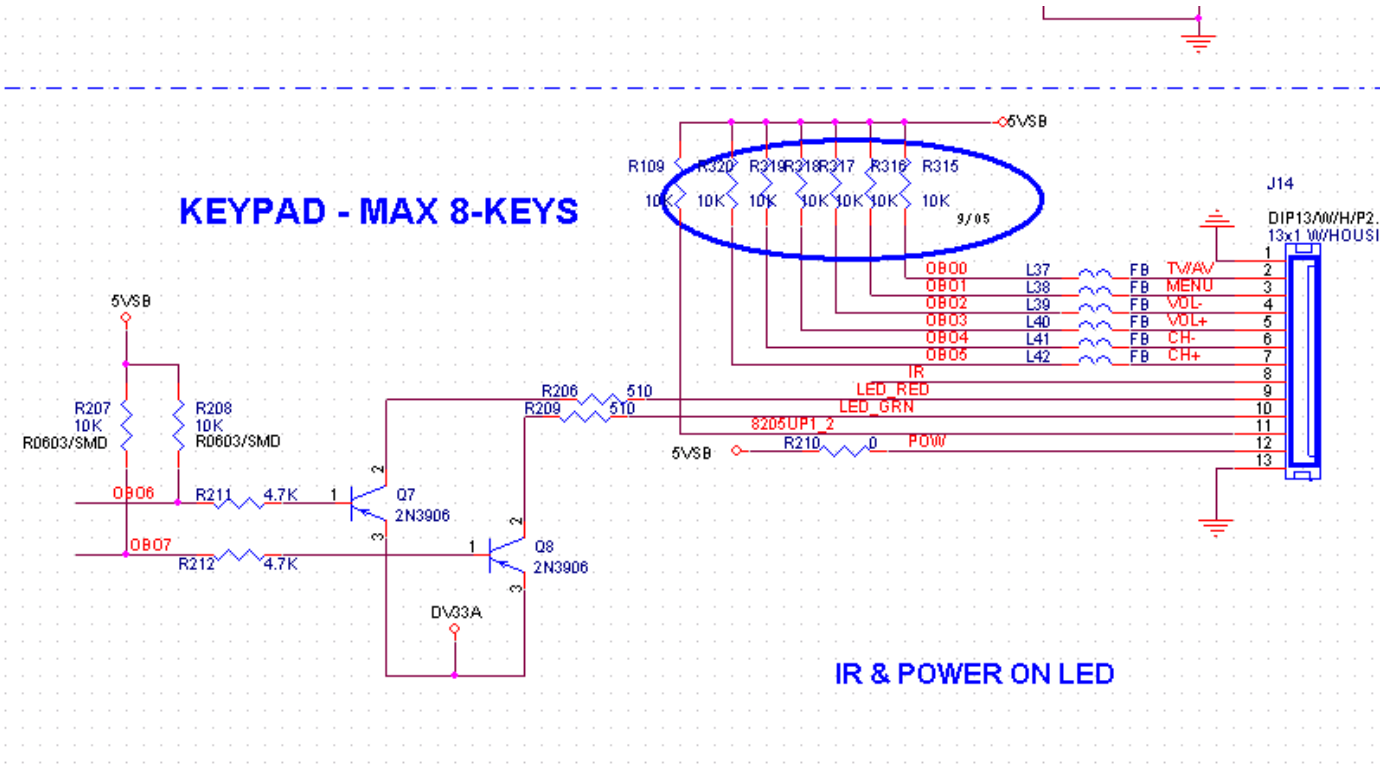

DF1
DF2
R181
R349
R348
R182
R113
CE46
R205
R199
R201
Q5
CB1
R337
C132
R3
R4
C133
R152
R369
T51
R370
R361
R301
R179
R180
R192
R296
R364
R189
R188
R297
R193
R194
R298
R295
R286
R185
R186
R187
Q4
U2
R371
Q17
U34
L34
CE49
CE47
CE48
CE41
CE2
F1

5.The remote control don’t be control.

6.1 The check batteries of remote control if it run out of .

6.2 To check main board of connecter J14 of wire connect fastness and the connecter of wire open.

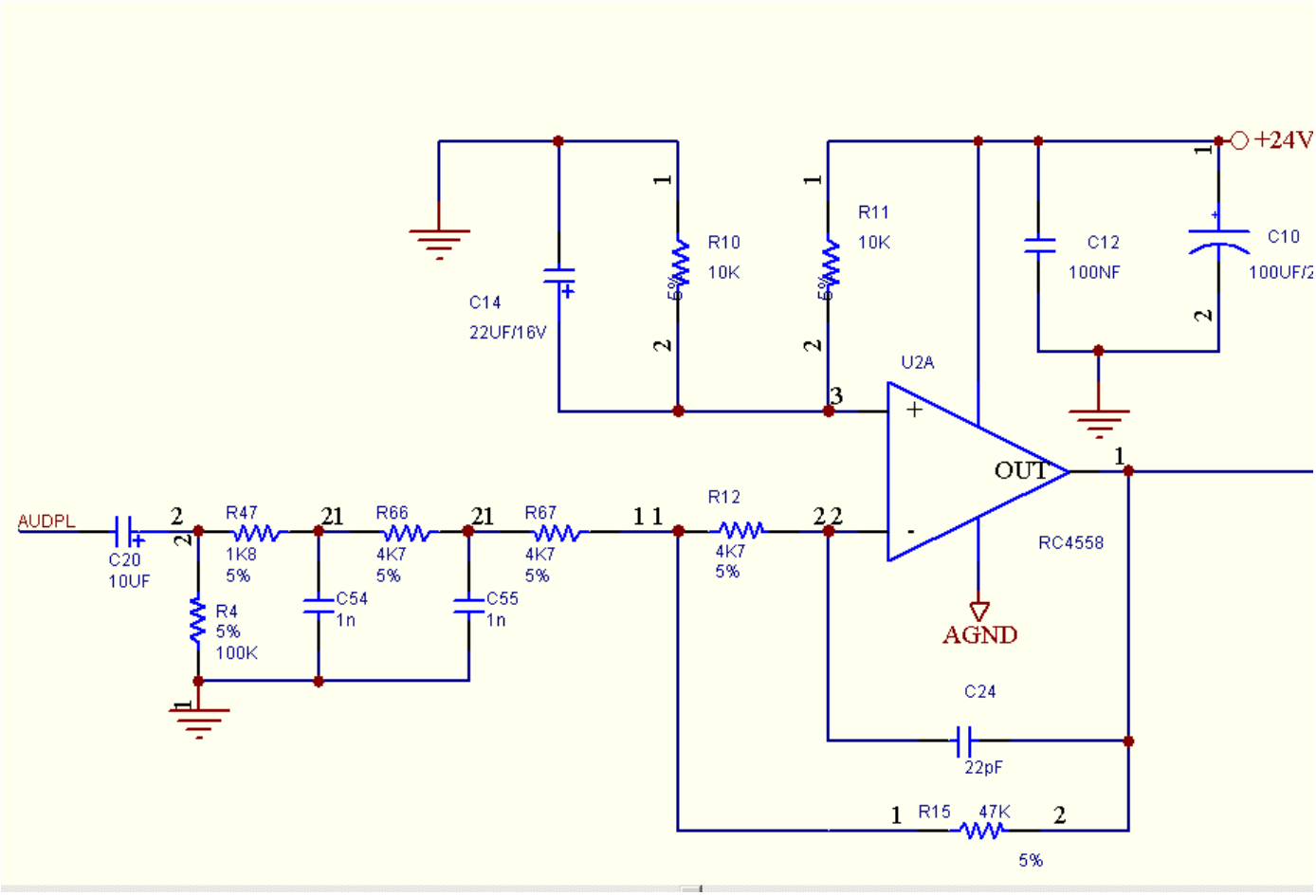
The circuit diagram follow down:



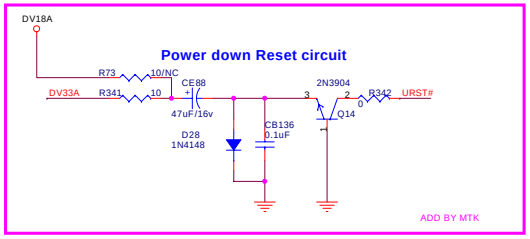
6.The sound don’t output.

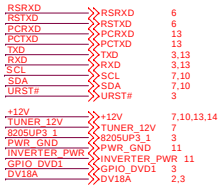
7.1 To check TV board +24v voltage ,It’s true not +24v voltage. Then check diode D11 if open and IC U1,U3 short

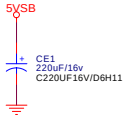
The circuit diagram follow down:

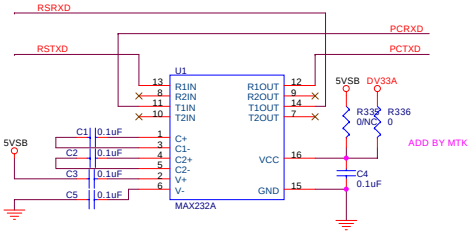


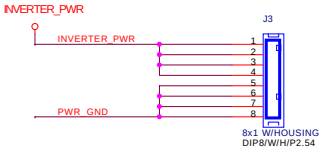
MT8205E (PBGA388) LCDTV BOARD 4 LAYERS

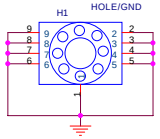


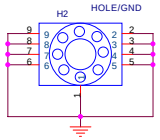


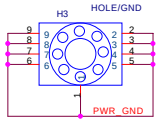


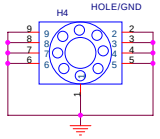


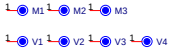


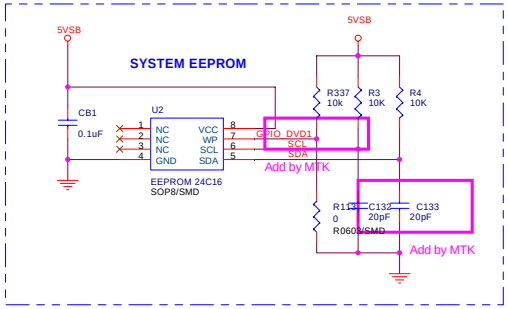


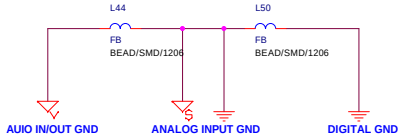


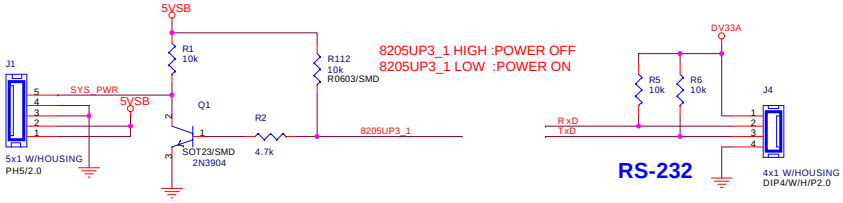


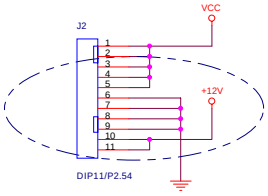


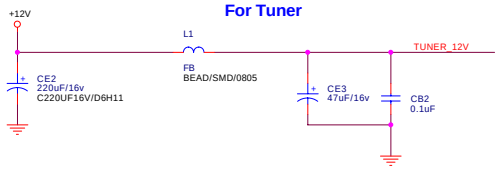


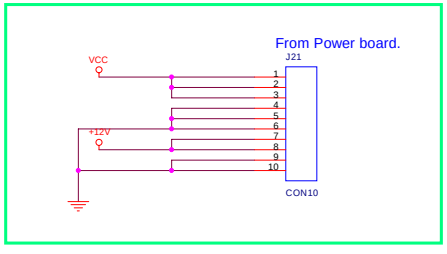












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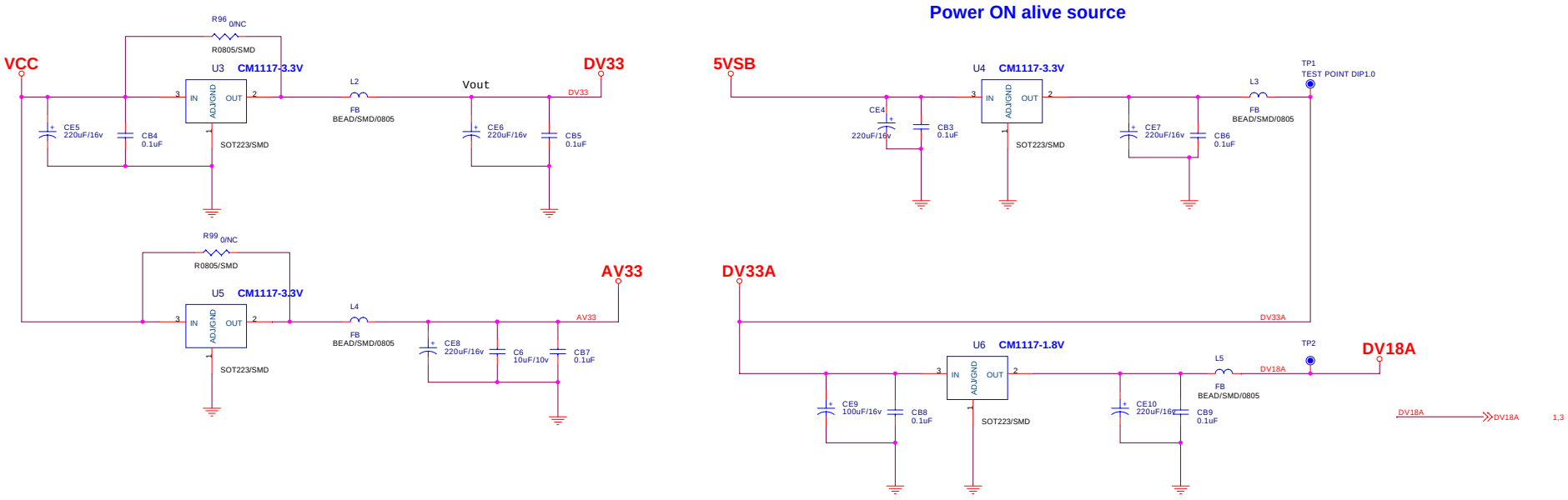
Title	MiCO LCD TV - MediaTek MT8205 Solution	
Size C	Doc Number INDEX	Rev V1.2
Date: Wednesday, October 19, 2005	Sheet 1 of 15	



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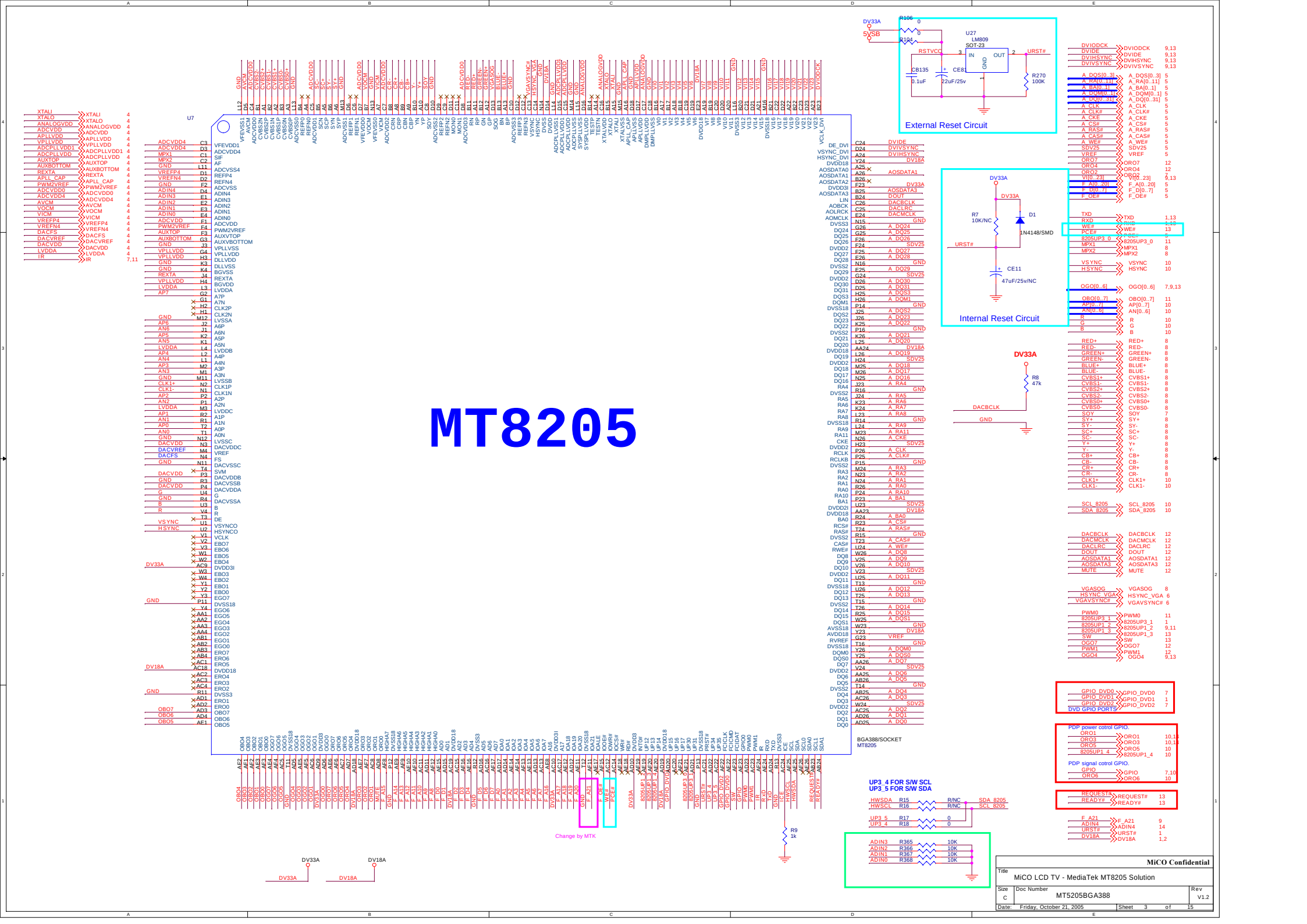
Title	MiCO LCD TV - MediaTek MT8205 Solution	
Size C	Doc Number LDO	Rev V1.2
Date: Wednesday, October 19, 2005	Sheet 2 of 15	


MT8205
External Reset Circuit
Internal Reset Circuit
BGA388/SOCKET
MT8205
Change by MTK
UP3_4 FOR S/W SCL
UP3_5 FOR S/W SDA
DV33A
DV18A
5VSB
DVD GPIO PORTS
PDP power cotrol GPIO.
PDP signal cotrol GPIO.
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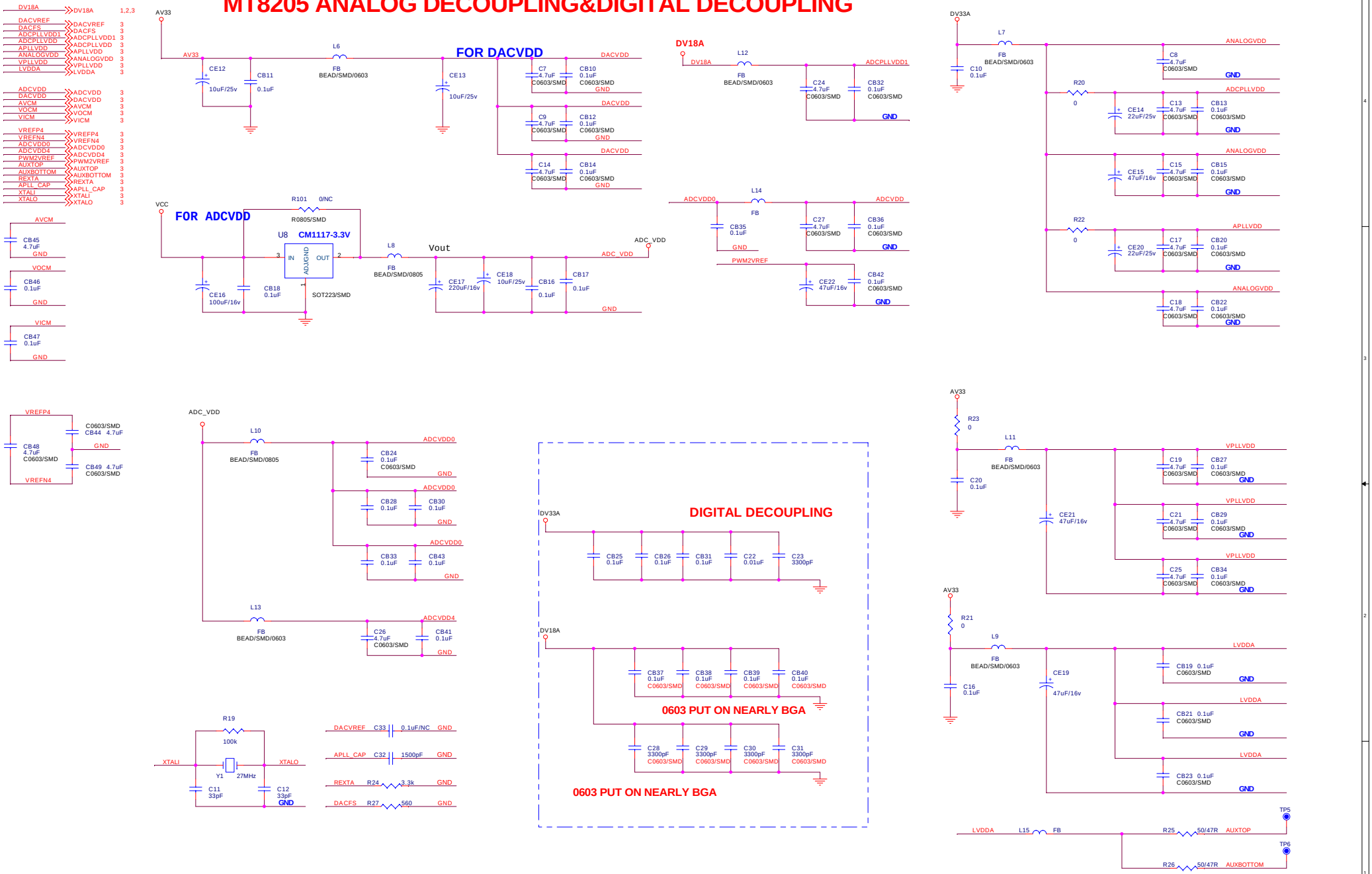
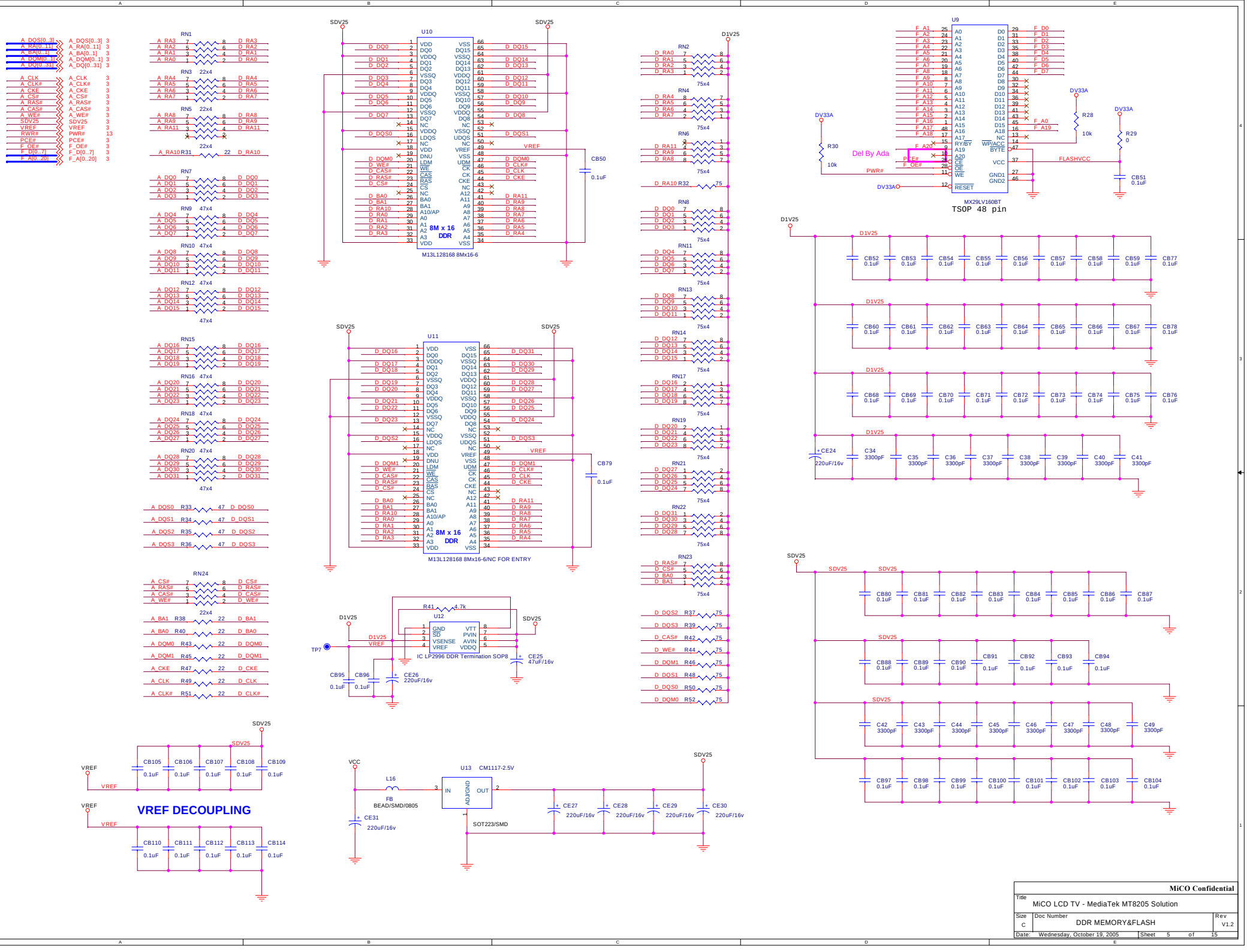
MiCO LCD TV - MediaTek MT8205 Solution
MT5205BGA388
Friday, October 21, 2005

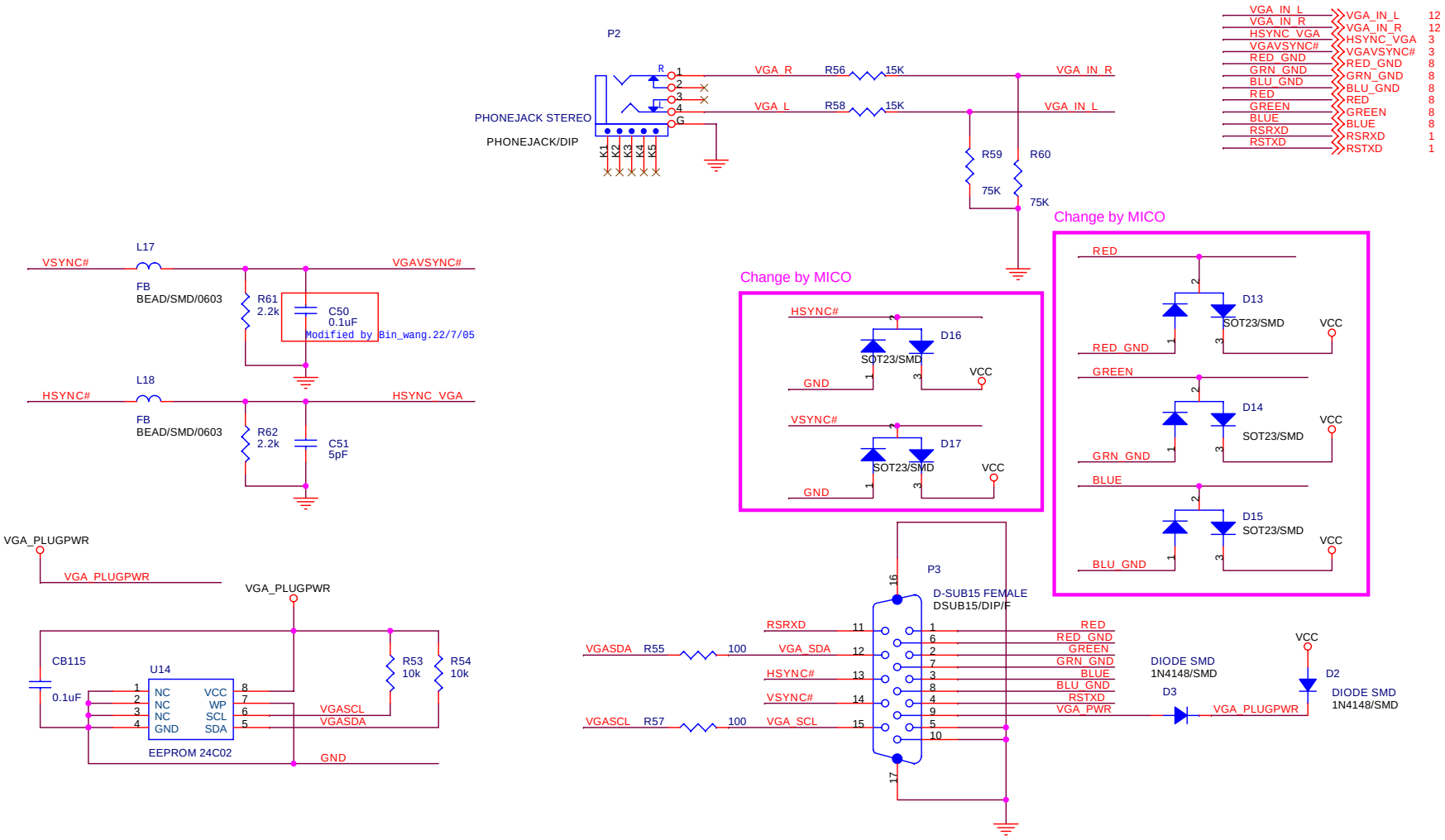
MT8205 ANALOG DECOUPLING&DIGITAL DECOUPLING



MiCO Confidential

Title	MiCO LCD TV - MediaTek MT8205 Solution	
Size C	Doc Number MT8205 DECOUPOMG--ANALOG	Rev V1.2
Date: Wednesday, October 19, 2005	Sheet 4 of 15	


A_DQS[0..3] 3
A_RA[0..11] 3
A_BA[0..1] 3
A_DQM[0..1] 3
A_DQ[0..31] 3
A_CLK 3
A_CLK# 3
A_CKE 3
A_CS# 3
A_RAS# 3
A_CAS# 3
A_WE# 3
SDV25 3
VREF 3
PWR# 13
PCE# 3
F_OE# 3
F_D[0..7] 3
F_A[0..20] 3
RN1
RN3 22x4
RN5 22x4
22x4
RN7
RN9 47x4
RN10 47x4
RN12 47x4
47x4
RN15
RN16 47x4
RN18 47x4
RN20 47x4
47x4
RN24
22x4
VREF DECOUPLING
U10
U11
8M x 16 DDR
M13L128168 8Mx16-6
M13L128168 8Mx16-6/NC FOR ENTRY
U12
IC LP2996 DDR Termination SOP8
U13 CM1117-2.5V
SOT223/SMD
FB BEAD/SMD/0805
RN2
RN4
RN6
RN8
RN11
RN13
RN14
RN17
RN19
RN21
RN22
RN23
75x4
U9
MX29LV160BT
TSOP 48 pin
Del By Ada
FLASHVCC
MiCO Confidential
MiCO LCD TV - MediaTek MT8205 Solution
DDR MEMORY&FLASH
Wednesday, October 19, 2005
Sheet 5 of 15
Rev V1.2



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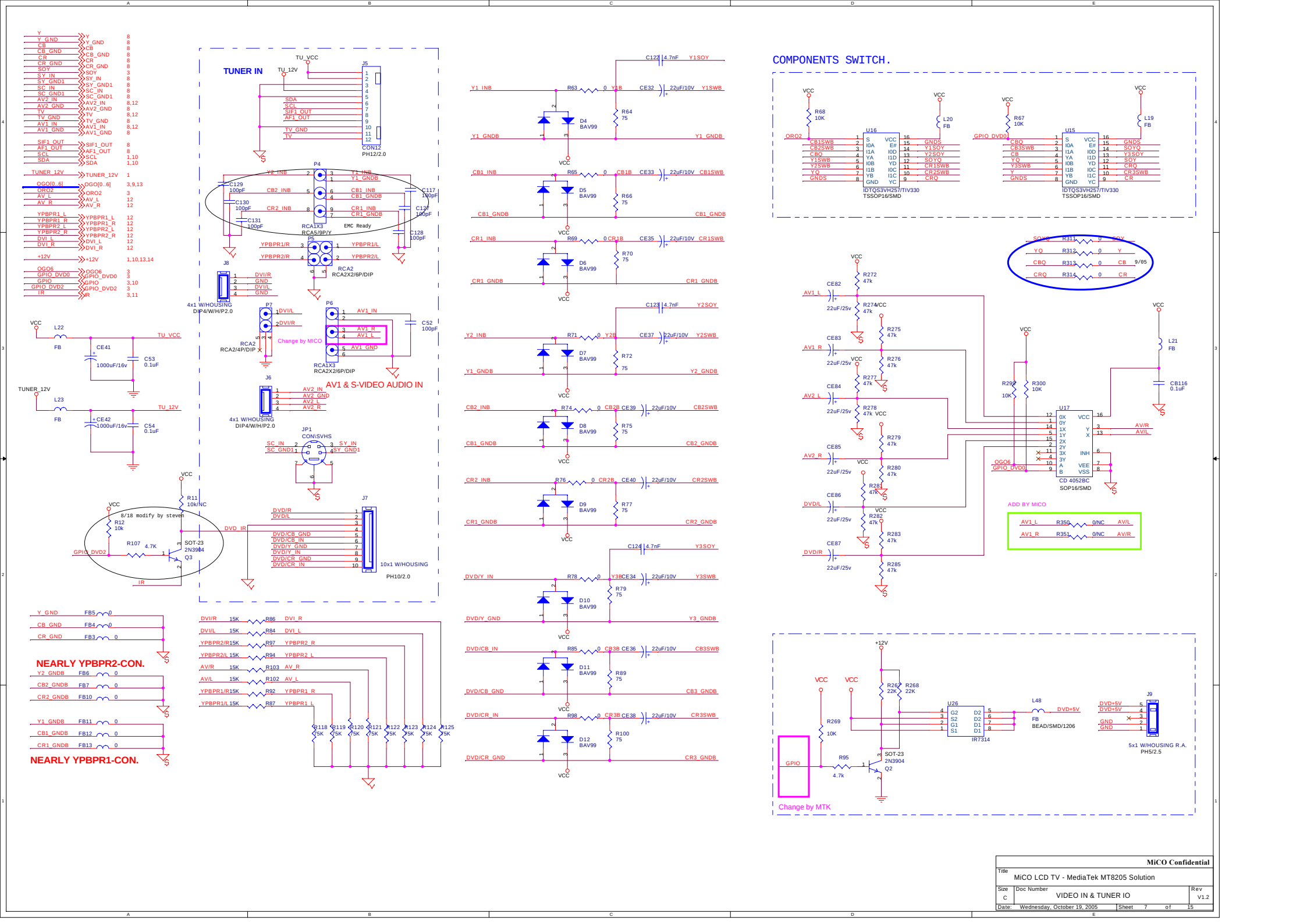
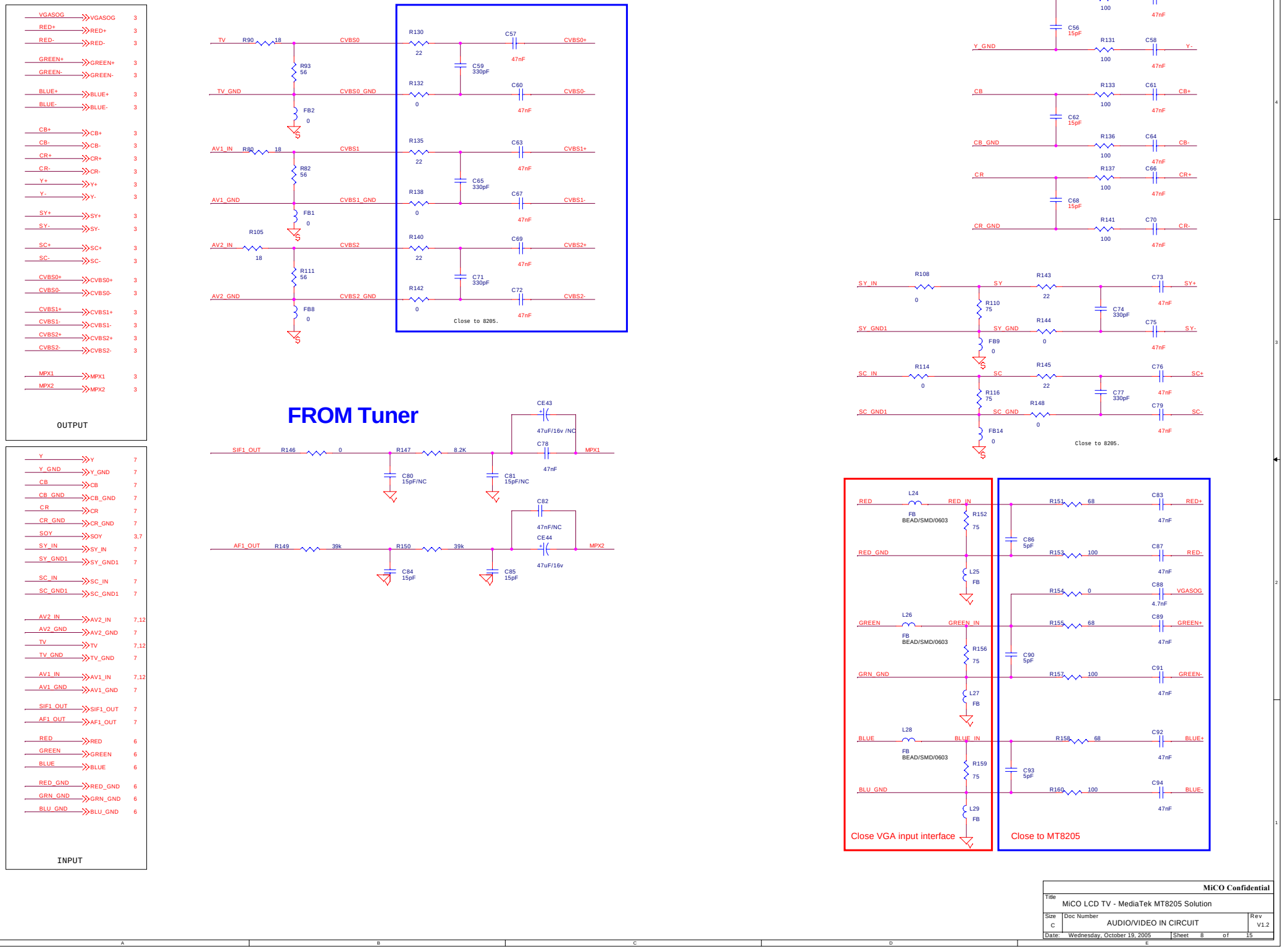
Title: MiCO LCD TV - MediaTek MT8205 Solution		
Size: B	Doc Number: VGA IN&PC AUDIO IN	Rev: V1.2
Date: Wednesday, October 19, 2005	Sheet 6 of 15	


TUNER IN
AV1 & S-VIDEO AUDIO IN
COMPONENTS SWITCH.
NEARLY YPBPR2-CON.
NEARLY YPBPR1-CON.
Change by MICO
Change by MTK
ADD BY MICO
8/18 modify by steven
MiCO Confidential
MiCO LCD TV - MediaTek MT8205 Solution
VIDEO IN & TUNER IO
Wednesday, October 19, 2005


VGASOG
RED+
RED-
GREEN+
GREEN-
BLUE+
BLUE-
CB+
CB-
CR+
CR-
Y+
Y-
SY+
SY-
SC+
SC-
CVBS0+
CVBS0-
CVBS1+
CVBS1-
CVBS2+
CVBS2-
MPX1
MPX2
OUTPUT
Y
Y_GND
CB
CB_GND
CR
CR_GND
SOY
SY_IN
SY_GND1
SC_IN
SC_GND1
AV2_IN
AV2_GND
TV
TV_GND
AV1_IN
AV1_GND
SIF1_OUT
AF1_OUT
RED
GREEN
BLUE
RED_GND
GRN_GND
BLU_GND
INPUT
TV R90 18 CVBS0 R130 22 C57 47nF CVBS0+
R93 56 C59 330pF
TV_GND CVBS0_GND R132 0 C60 47nF CVBS0-
FB2 0
AV1_IN R89 18 CVBS1 R135 22 C63 47nF CVBS1+
R82 56 C65 330pF
AV1_GND CVBS1_GND R138 0 C67 47nF CVBS1-
FB1 0
R105
AV2_IN 18 CVBS2 R140 22 C69 47nF CVBS2+
R111 56 C71 330pF
AV2_GND CVBS2_GND R142 0 C72 47nF CVBS2-
FB8 0
Close to 8205.
FROM Tuner
SIF1_OUT R146 0 R147 8.2K CE43 47uF/16v /NC C78 47nF MPX1
C80 15pF/NC C81 15pF/NC
C82 47nF/NC
AF1_OUT R149 39k R150 39k CE44 47uF/16v MPX2
C84 15pF C85 15pF
Y R128 100 C55 47nF Y+
C56 15pF
Y_GND R131 100 C58 47nF Y-
CB R133 100 C61 47nF CB+
C62 15pF
CB_GND R136 100 C64 47nF CB-
CR R137 100 C66 47nF CR+
C68 15pF
CR_GND R141 100 C70 47nF CR-
SY_IN R108 0 SY R143 22 C73 47nF SY+
R110 75 C74 330pF
SY_GND1 SY_GND R144 0 C75 47nF SY-
FB9 0
SC_IN R114 0 SC R145 22 C76 47nF SC+
R116 75 C77 330pF
SC_GND1 SC_GND R148 0 C79 47nF SC-
FB14 0
Close to 8205.
RED L24 RED_IN R151 68 C83 47nF RED+
FB BEAD/SMD/0603 R152 75
C86 5pF
RED_GND R153 100 C87 47nF RED-
L25 FB
R154 0 C88 4.7nF VGASOG
GREEN L26 GREEN_IN R155 68 C89 47nF GREEN+
FB BEAD/SMD/0603 R156 75
C90 5pF
GRN_GND R157 100 C91 47nF GREEN-
L27 FB
BLUE L28 BLUE_IN R158 68 C92 47nF BLUE+
FB BEAD/SMD/0603 R159 75
C93 5pF
BLU_GND R160 100 C94 47nF BLUE-
L29 FB
Close VGA input interface
Close to MT8205
MiCO Confidential
Title
MiCO LCD TV - MediaTek MT8205 Solution
Size C
Doc Number AUDIO/VIDEO IN CIRCUIT
Rev V1.2
Date: Wednesday, October 19, 2005
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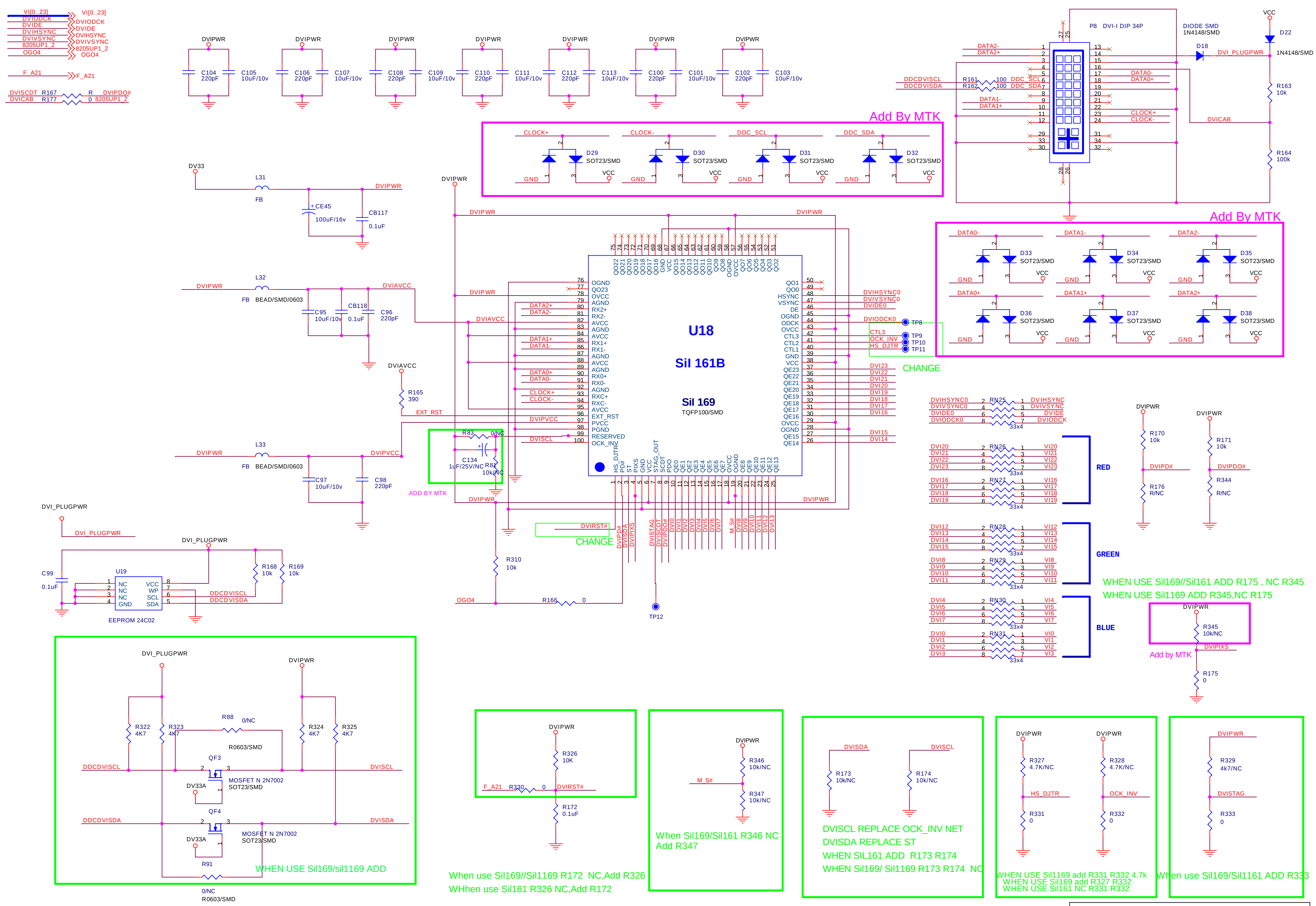

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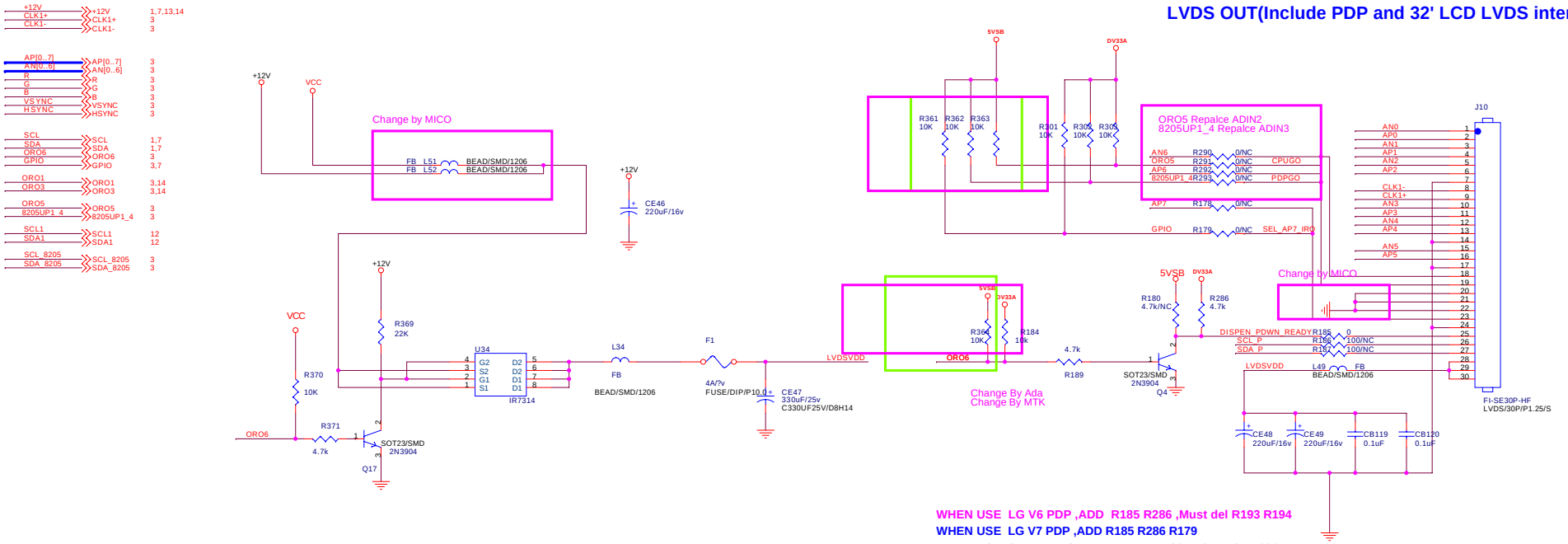
Title	MiCO LCD TV - MediaTek MT8205 Solution	
Size C	Doc Number DVI INPUT	Rev V1.2
Date: Friday, October 21, 2005	Sheet 9 of 15	

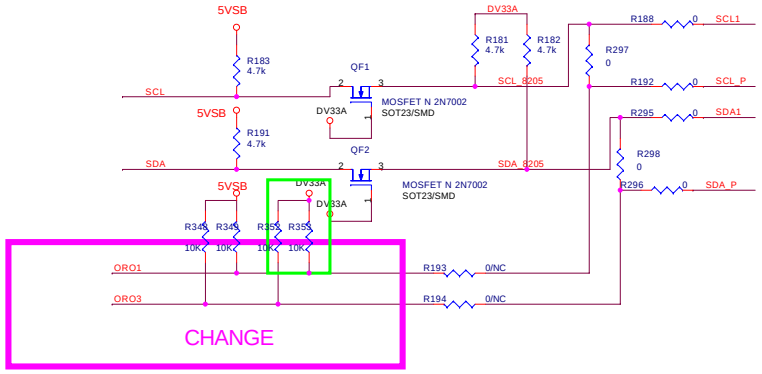
LVDS OUT(Include PDP and 32' LCD LVDS interface)

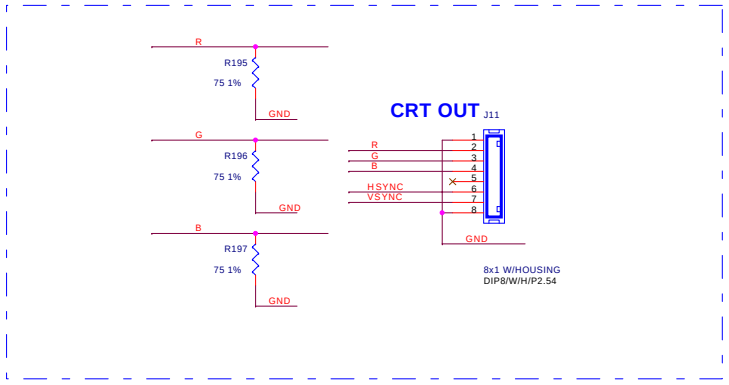


WHEN USE LG V6 PDP ,ADD R185 R286 ,Must del R193 R194
WHEN USE LG V7 PDP ,ADD R185 R286 R179
WHEN USE SangsungSD1 PDP ,ADD R186 R187 R185 R286
WHEN USE Fujitsu 42 PDP ,ADD R179 R186 R187 R185 R286 R291 R293.REMOVE R178 R290 R292

WHEN NOT USE PDP ADD L49 R178 R290 R292
REMOVE R179 R185 R186 R187 R291 R293

4.7K REPALAC 47K





MiCO Confidential		
Title: MiCO LCD TV - MediaTek MT8205 Solution		
Size: C	Doc Number: LVDS/CRT OUT	Rev: V1.2
Date: Wednesday, October 19, 2005	Sheet 10 of 15	

OBO[0..7] → OBO[0..7] 3

IR → IR 3,7
PWR_GND → PWR_GND 1
INVERTER_PWR → INVERTER_PWR 1

OBO0 → OBO0 3
OBO1 → OBO1 3
OBO2 → OBO2 3
OBO3 → OBO3 3
OBO4 → OBO4 3
OBO5 → OBO5 3
OBO6 → OBO6 3
OBO7 → OBO7 3
8205UP3_0 → 8205UP3_0 3
PWM0 → PWM0 3,14
8205UP1_2 → 8205UP1_2 3,9
PWR_GND → PWR_GND 1

PANEL INVERTER POWER

Inverter_PWR — CE50 470uF/50v — CE51 470uF/50v — CB121 0.1uF — CB122 0.1uF — Inverter_PWR
PWR_GND

FOR AU 32" INVERTER CONNECTOR

VCC
R199 10k
PWM0 — R201 4.7k — Q5 2N3904 SOT23/SMD
R200 100k
CB123 0.1uF
Dimming
Inverter_PWR
PWR_GND
J12 — 14x1 W/HOUSING DIP14/WH/P2.0/R — R. ANGLE
SELECT
VCC
R202 R
R204 0

External PWM input for dimming control

Back Light circuit

VCC
R203 10k
BL_ON/OFF
8205UP3_0 — R205 4.7k — Q6 2N3904 SOT23/SMD

Inverter_PWR
PWR_GND
J13 — 10x1 W/HOUSING R.A. DIP10/WH/P2.0/R — R. ANGLE
L35 FB BEAD/SMD/1206
L36 FB BEAD/SMD/1206

KEYPAD - MAX 8-KEYS

5VSB
R109 10K — R320 10K — R216 10K — R217 10K — R218 10K — R317 10K — R315 10K
9/05

J14 — DIP13/W/H/P2.0 13x1 W/HOUSING

OBO0 — L37 FB — TV/AV
OBO1 — L38 FB — MENU
OBO2 — L39 FB — VOL-
OBO3 — L40 FB — VOL+
OBO4 — L41 FB — CH-
OBO5 — L42 FB — CH+
IR
LED_RED
LED_GRN
8205UP1_2
5VSB — R210 0 — POW

5VSB
R207 10K R0603/SMD
R208 10K R0603/SMD
OBO6 — R211 4.7K — Q7 2N3906
OBO7 — R212 4.7K — Q8 2N3906
R206 510
R209 510
DV33A

IR & POWER ON LED

J19 — CON9
TV/AV
MENU
VOL-
VOL+
CH-
CH+
8205UP1_2

J20 — CONN RCPT 5
IR
LED_RED
LED_GRN
POW

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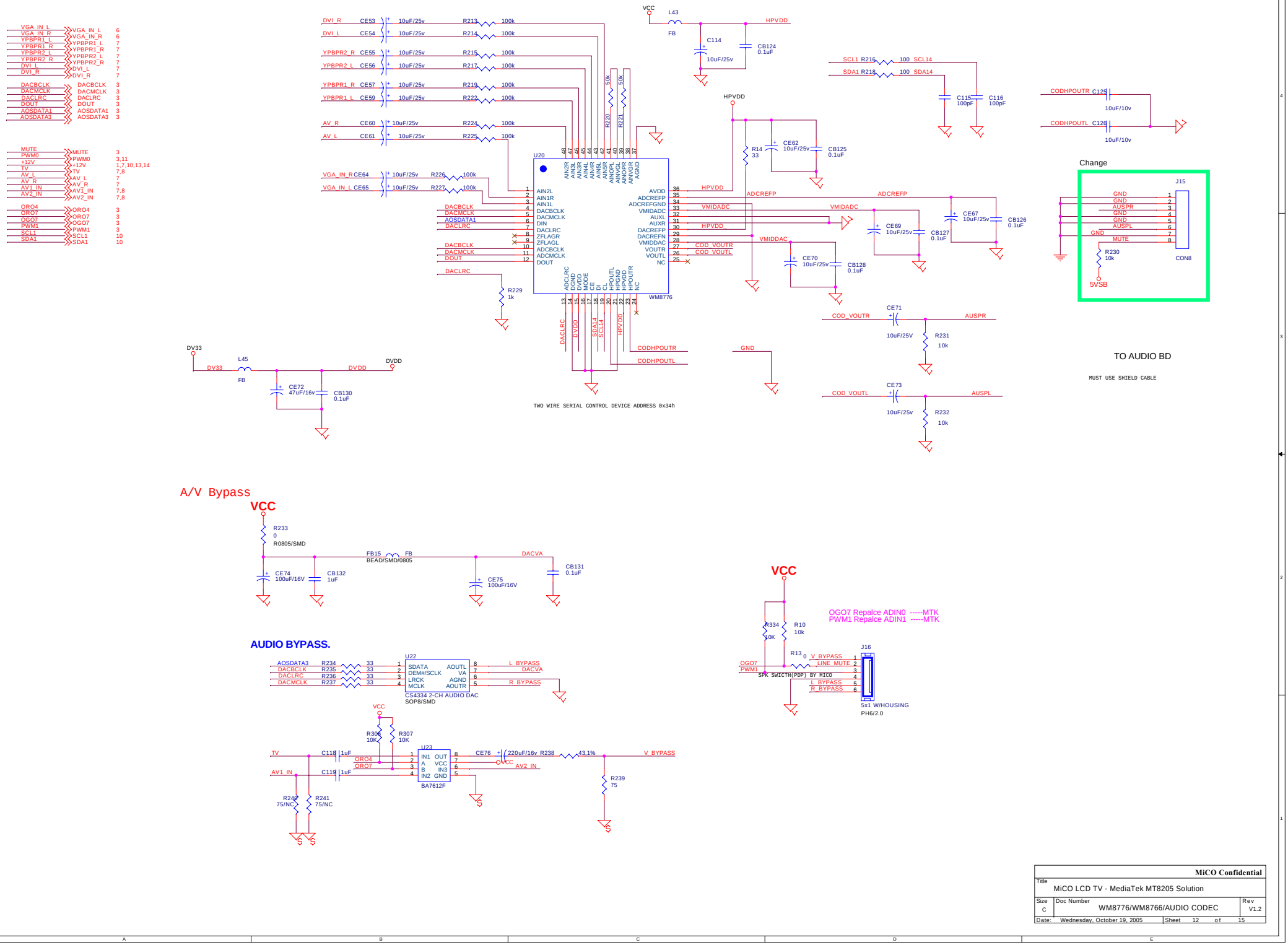
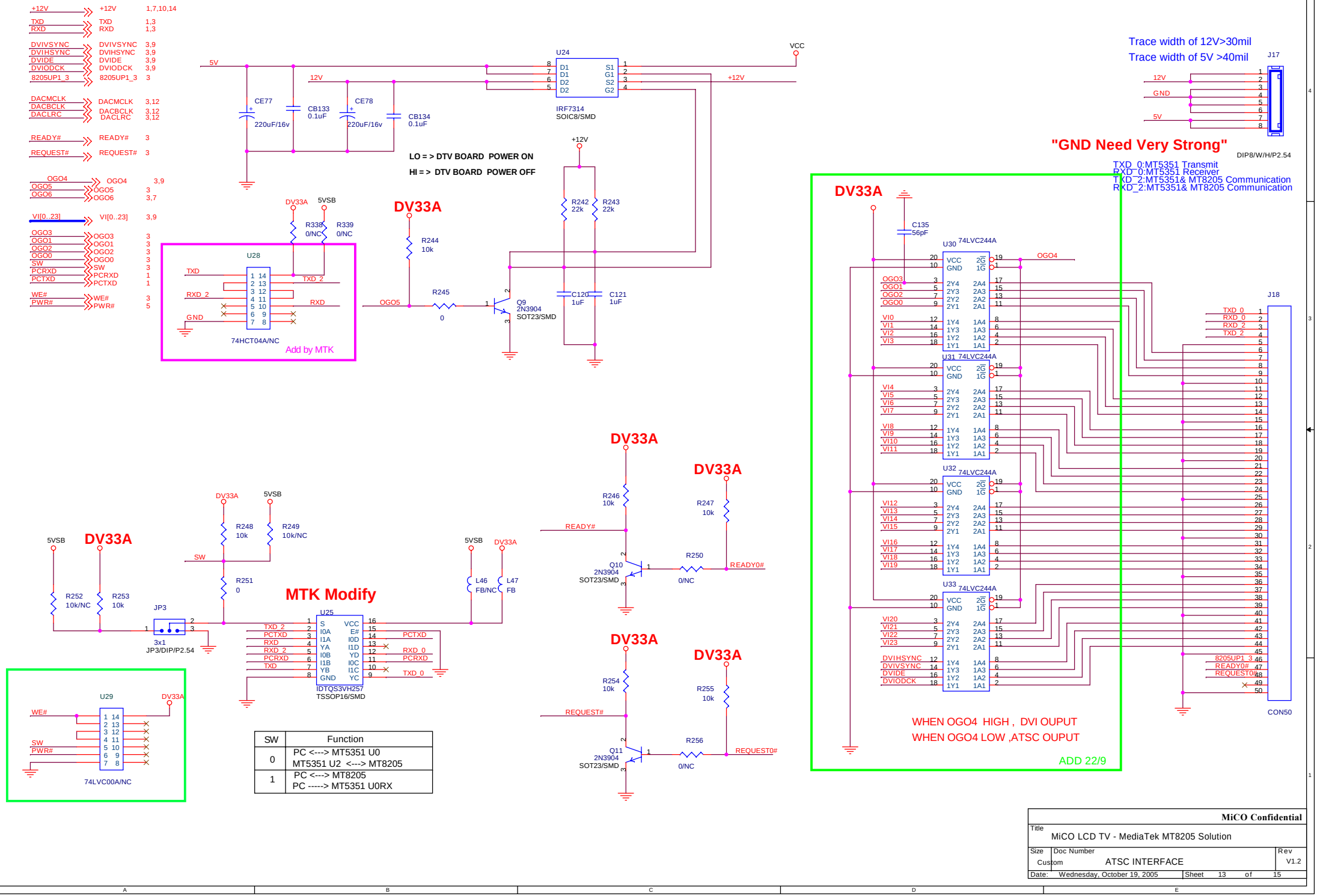
Title	MiCO LCD TV - MediaTek MT8205 Solution	
Size C	Doc Number BACK_LIGHT/KEYPAD	Rev V1.2
Date: Wednesday, October 19, 2005	Sheet 11 of 15	



MiCO Confidential

Title	MiCO LCD TV - MediaTek MT8205 Solution	
Size C	Doc Number WM8776/WM8766/AUDIO CODEC	Rev V1.2
Date: Wednesday, October 19, 2005	Sheet 12 of 15	



SW	Function
0	PC <---> MT5351 U0 MT5351 U2 <---> MT8205
1	PC <---> MT8205 PC -----> MT5351 U0RX

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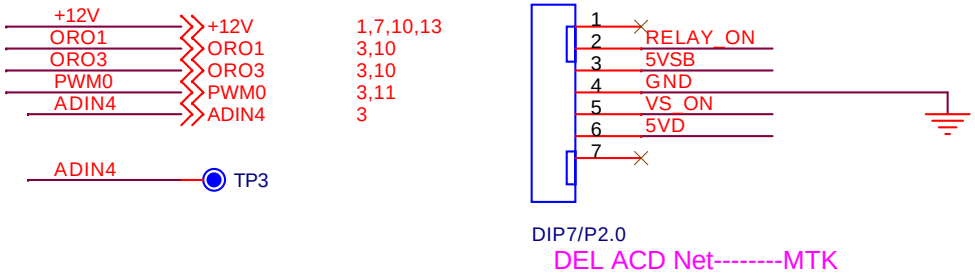
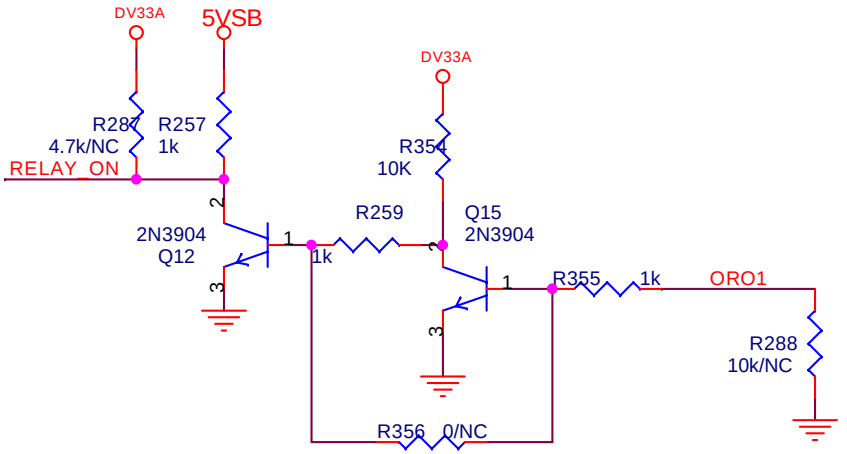
Title: MiCO LCD TV - MediaTek MT8205 Solution		
Size: Custom	Doc Number: ATSC INTERFACE	Rev: V1.2
Date: Wednesday, October 19, 2005	Sheet 13 of 15	

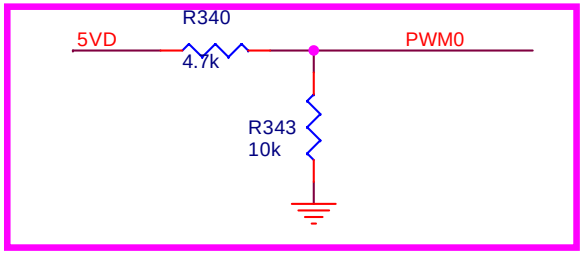


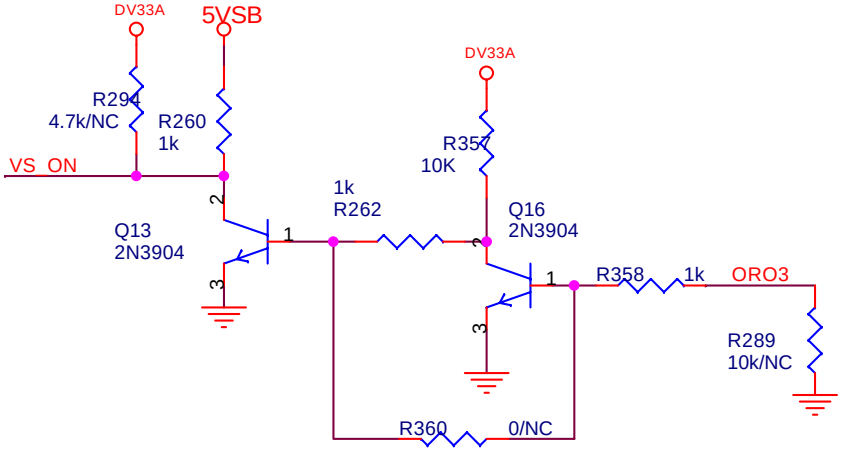
DEL ACD Net--------MTK



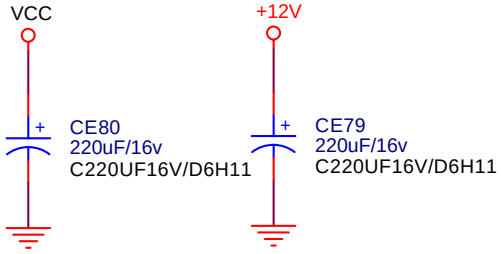
USE WHEN LG V6

Change--------MTK





USE WHEN LG V6



MiCO Confidential

Title: MiCO LCD TV - MediaTek MT8205 Solution		
Size: A	Doc Number: PDP interface	Rev: V1.2
Date: Wednesday, October 19, 2005	Sheet 14 of 15	

From V0.1 To V1.2 change item:

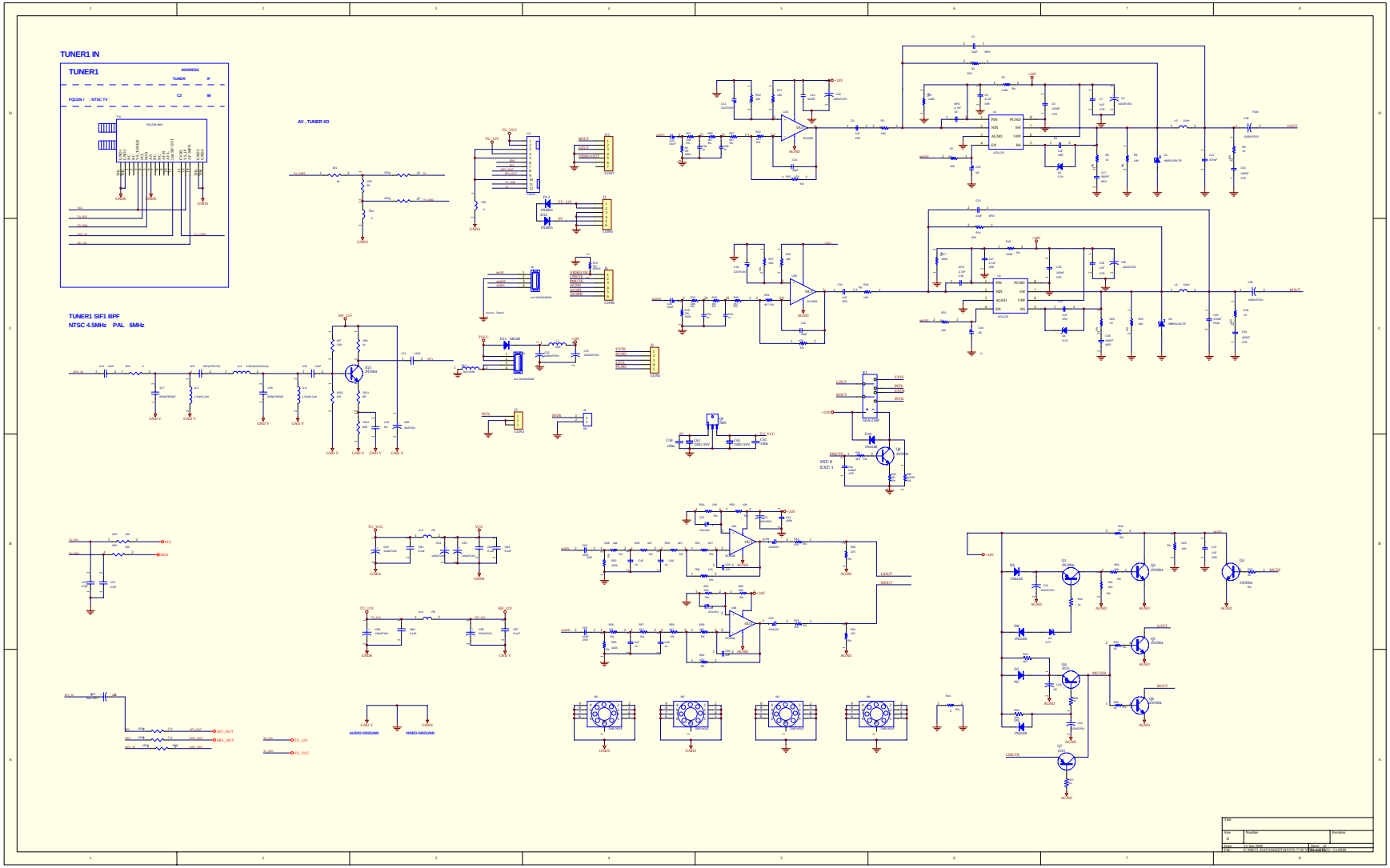
1,Add R109-10K;R107-4.7K;C135-56pF;0603-R88,R91,R104,R106-0欧姆.0805-R96,R99,R101-0欧姆

2,Reset IC 增加5V Supply;DVI AUDIO ADD CONNECTOR J8.

3,ADIN4 CHANGE TO PWM0

4,ADD UP3_1 PULL HIGH R112 10K

5,ADD R113 0R


TUNER1 IN
TUNER1
ADDRESS
TUNER IF
FQ1256 / NTSC TV C2 R6
AV , TUNER I/O
TUNER1 SIF1 BPF
NTSC 4.5MHz PAL 6MHz
AUDIO GROUND
VIDEO GROUND

TFT LCD Approval Specification

MODEL NO.: V320B1 - L01

Customer: _____

Approved by: _____

Note:

LCD TV Head Division	
AVP	郭振隆

QRA Dept.	TVHD / PDD		
	DDIII	DDII	DDI
Approval	Approval	Approval	Approval
陳永一	李汪洋	藍文錦	林文聰

LCD TV Marketing and Product Management Division	
Product Manager	徐子祥 陳立宜

- CONTENTS -

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 1.0	July 12,'04	All	All	Preliminary Specification was first issued.
		All	All	Approval Specification was first issued.
Ver 2.0	Sep. 15 ,'04	9	3.2.2	Input Voltage Min. : 21.6 → 22.8 Max. : 26.4 → 25.2 Input Ripple Noise Note : V_{BL}=21.6V → V_{BL}=22.8V
		12	4.1	Inverter connector CN1 : S10B-PH-SM3-TB(JST) → S10B-PH-SM3-TB(D)(LF)(JST) CN2 : S12B-PH-SM3-TB(JST) → S12B-PH-SM3-TB(D)(LF)(JST) CN3-CN10:SM02 (8.0)B-BHS-1-TB(JST) → SM02 (8.0)B-BHS-1-TB(LF)(JST) CN11: S2B-ZR-SM3A-TF (JST) → S2B-ZR-SM3A-TF (D)(LF)(JST)
		14	5.2	Inverter connectors are modified as Section 4.1. The Drawing is modified to a detail one.
		15	5.3	Inverter connectors are modified as Section 4.1.
		22	7.1	Oscillating Frequency (Inverter) : 62 ± 3 → 62.5 ± 3 Color Chromaticity : Min / Typ / Max Rx : 0.618 → 0.621 / 0.648 → 0.651 / 0.678 → 0.681 Gx : 0.242 → 0.239 / 0.272 → 0.269 / 0.302 → 0.299 Gy : 0.576 → 0.567 / 0.606 → 0.597 / 0.636 → 0.627 By : 0.044 → 0.036 / 0.074 → 0.066 / 0.104 → 0.096
		30	11	The Drawing is modified.
		31	11	The Drawing is modified.
Ver 2.1	Dec. 20 ,'04	4	1.2	Contrast Ratio : 800:1 →1000:1
		4	1.5	Weight : Min 5900→5700, Typ. 6100→5900, Max. 6300→6100
		7	3.1	Rush Current : Max. 1.7→3
		9	3.2.2	Oscillating Frequency : Min. 59.5 → 61.5,Max. 65.5→63.5
		13	5.1	CNF1 Connector Pin Assignment : Pin3 is modified.
		17	5.5	LVDS INTERFACE is modified.
		22	7.2	Contrast Ratio : Min.600 → 800,Typ. 800→1000 Response Time is modified. Color Chromaticity : Min / Typ / Max Rx : 0.621 → 0.622 / 0.651 → 0.652 / 0.681 → 0.682 Gx : 0.239 → 0.240 / 0.269 → 0.270 / 0.299 → 0.300 Gy : 0.567 → 0.559 / 0.597 → 0.589 / 0.627 → 0.619 Bx : 0.111 → 0.036 / 0.141 → 0.066 / 0.171 → 0.096 By : 0.036 → 0.038 / 0.066 → 0.068 / 0.096 → 0.098 Note are modified.
		30	11	The Drawing is modified.
		31	11	The Drawing is modified.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V320B1- L01 is a 32" TFT Liquid Crystal Display module with 16-CCFL Backlight unit and 1ch-LVDS interface. This module supports 1366 x 768 WXGA format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

-High brightness (550 nits)

- High contrast ratio (1000:1)
- Fast response time
- High color saturation NTSC 75%
- WXGA (1366 x 768 pixels) resolution
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 50/60 Hz frame rate
- Ultra wide viewing angle : 176(H)/176(V) (CR>20) Super MVA technology
- 180 degree rotation display option

1.3 APPLICATION

- TFT LCD TVs

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	708.954(H) x 398.592 (V) (32.02" diagonal)	mm	(1)
Bezel Opening Area	714.96 (H) x 404.6 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1366 x R.G.B. x 768	pixel	
Pixel Pitch (Sub Pixel)	0.1730 (H) x 0.5190 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	16.7M	color	
Display Operation Mode	Transmissive mode / Normally black	-	
Surface Treatment	Hardness : 3H, Haze : 40% Anti-reflective coating < 2% reflection	-	

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	759.25	760	760.75	mm	
	Vertical(V)	449.25	450	450.75	mm	
	Depth(D)	37.45	37.95	38.75	mm	To PCB cover
	Depth(D)	46.53	47.53	48.53	mm	To inverter cover
Weight		5700	5900	6100	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

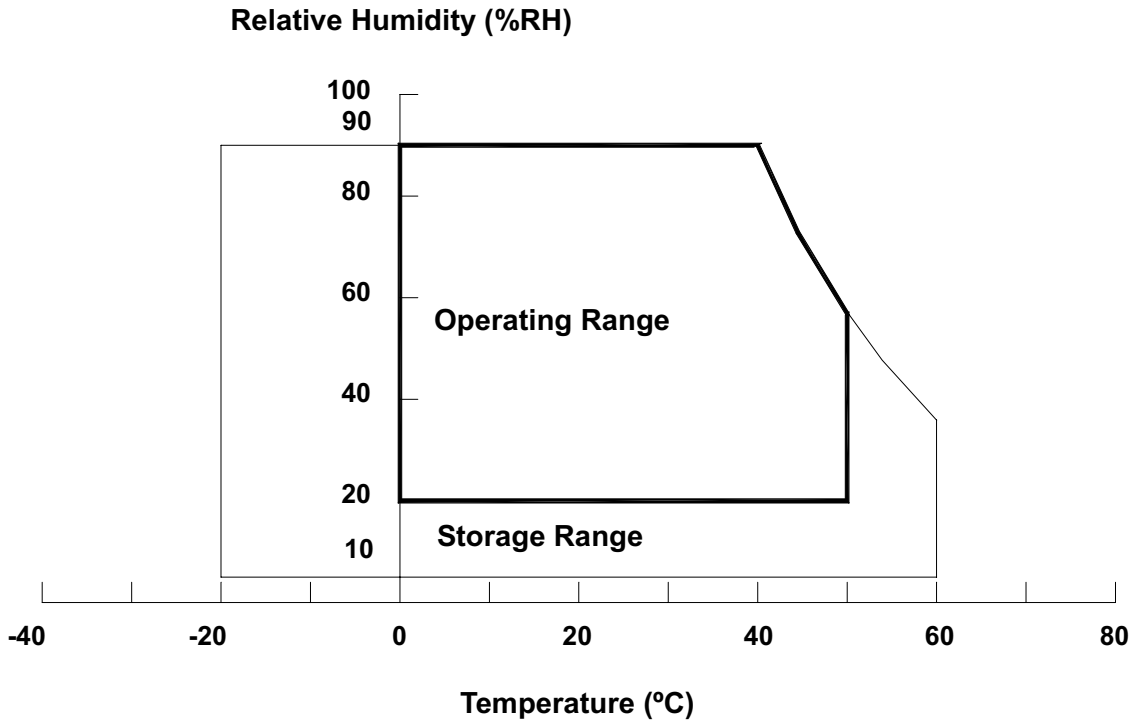
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 60 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 60 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	6.0	V	(1)
Input Signal Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	3000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals includes Backlight On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

3. ELECTRICAL CHARACTERISTICS

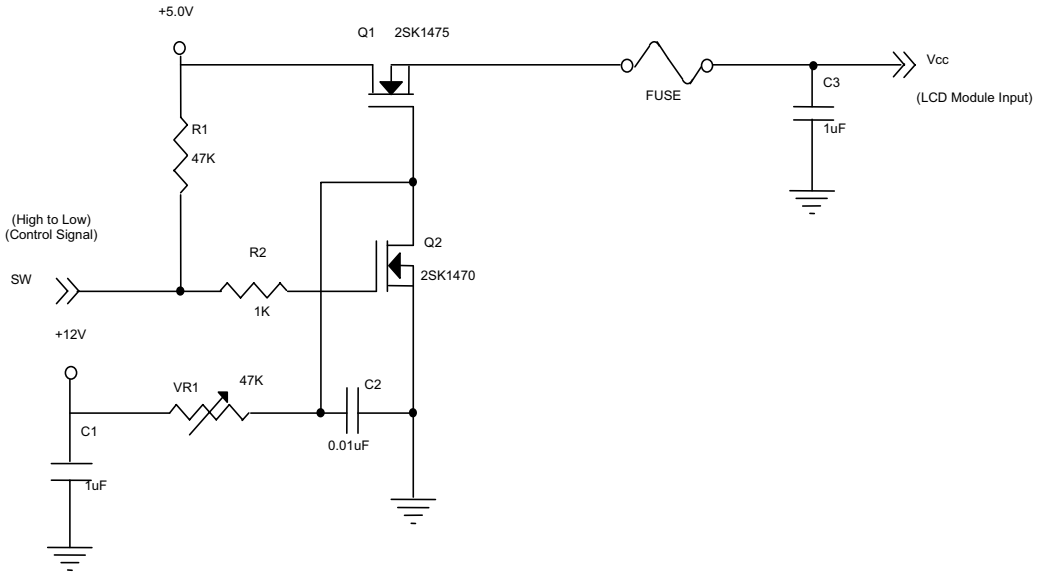
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

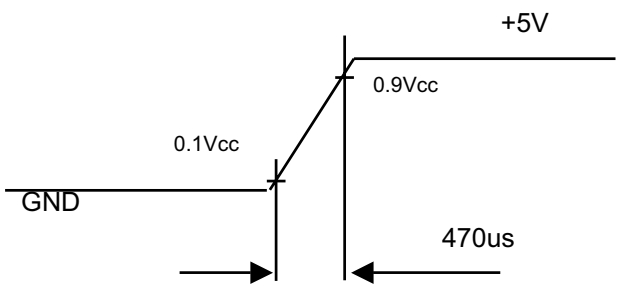
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	4.5	5.0	5.5	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	100	mV	
Rush Current		I_{RUSH}	-	-	3.0	A	(2)
Power Supply Current	White	I_{CC}	-	1.48	-	A	(3)
	Black		-	0.85	-	A	
	Vertical Stripe		-	1.23	-	A	
LVDS Interface	Differential Input High Threshold Voltage	V_{LVTH}	-	-	+100	mV	
	Differential Input Low Threshold Voltage	V_{LVTL}	-100	-	-	mV	
	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:

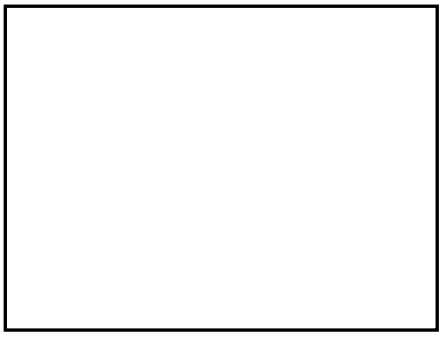


Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 5 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

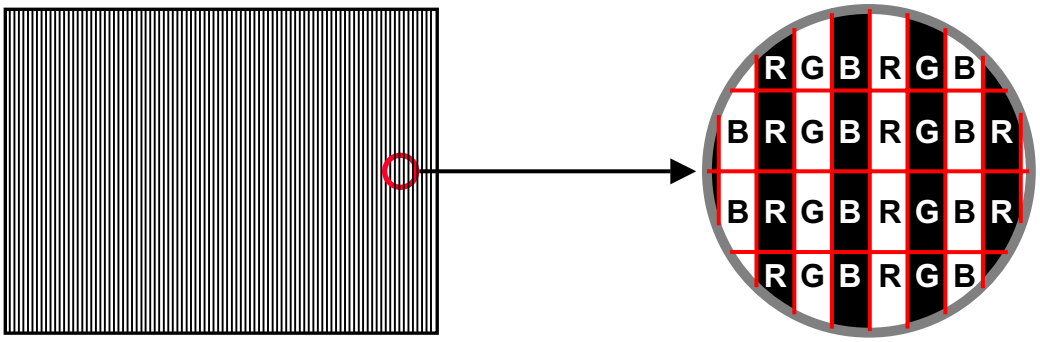


Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT INVERTER UNIT

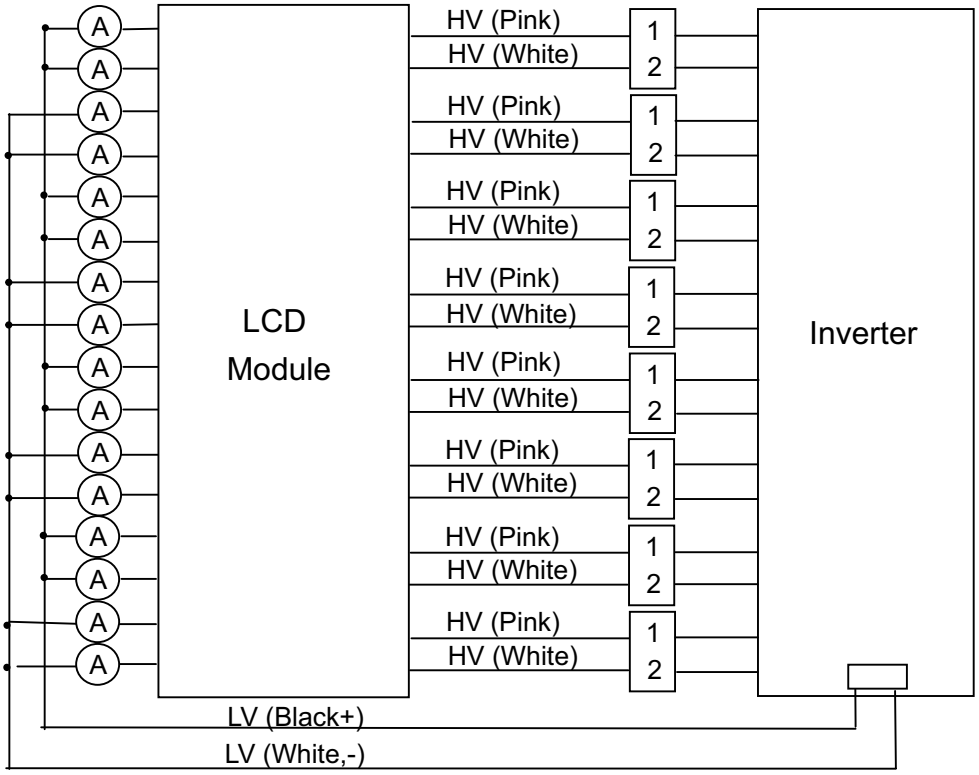
3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	V_W	-	1280	-	V_{RMS}	I_L = 4.5mA
Lamp Current	I_L	4.0	4.5	5.0	mA_{RMS}	(1)
Lamp Starting Voltage	V_S	-	-	2450	V_{RMS}	(2), Ta = 0 ºC
		-	-	2360	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_O	40	-	70	KHz	(3)
Lamp Life Time	L_{BL}	50,000	60,000	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	103	-	W	(5),(6), I_L = 4.5mA
Input Voltage	V_{BL}	22.8	24	25.2	V_{DC}	
Input Current	I_{BL}	-	4.3	-	A	Non Dimming
Input Ripple Noise	-	-	-	500	mV_{P-P}	V_{BL}=22.8V
Backlight Turn on Voltage	V_{BS}	2450	-	-	V_{RMS}	Ta = 0 ºC
		2360	-	-	V_{RMS}	Ta = 25 ºC
Oscillating Frequency	F_W	61.5	62.5	63.5	kHz	
Dimming frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second under starting up duration. Otherwise the lamp could not be lighted on completed.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the

condition at Ta = 25 ±2℃ and I_L = 4.0 ~ 5.0 mA_{RMS}.

Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

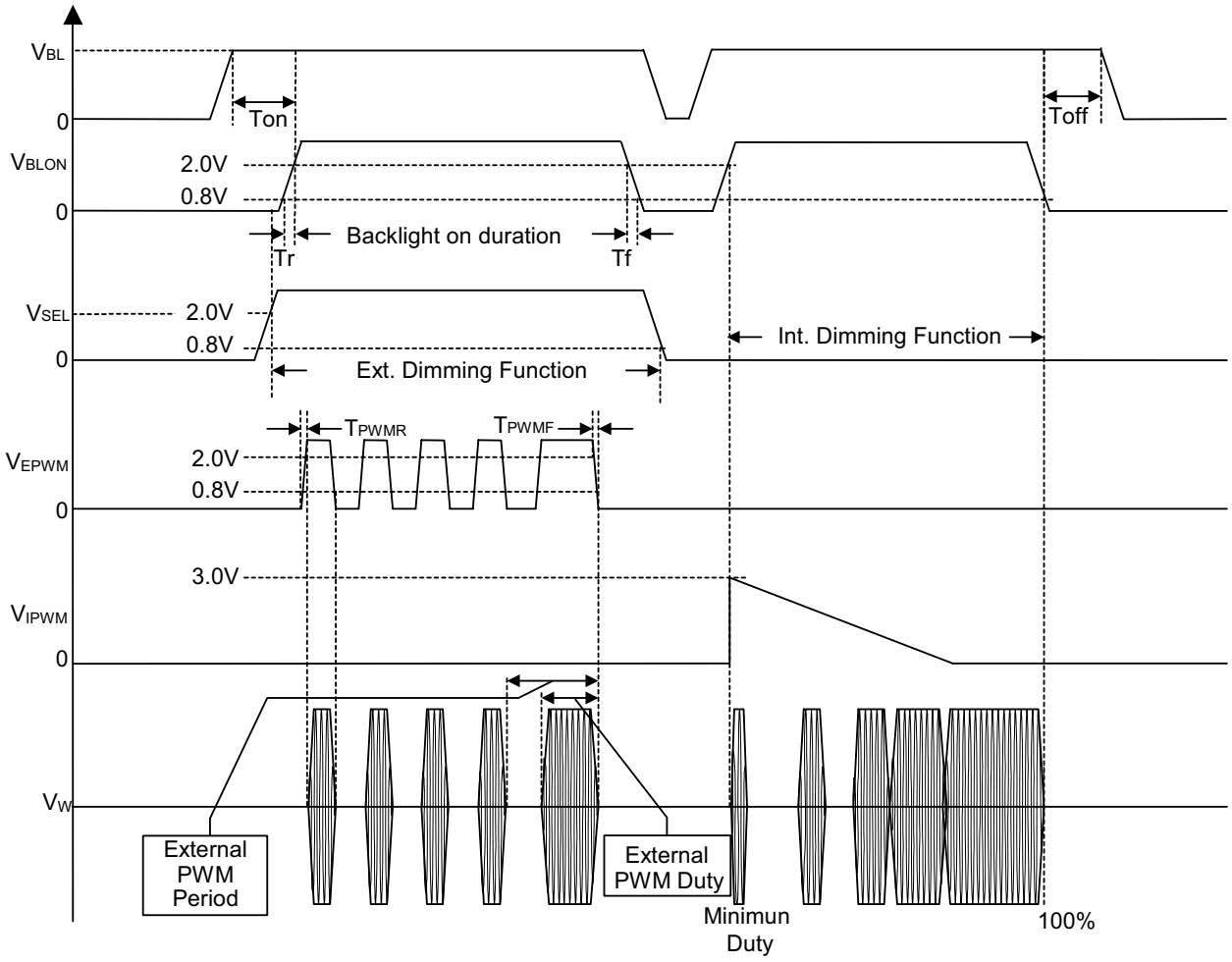
Note (6) To enhance the performance of backlight, the power consumption will increase to 1.5 times of the typical power consumption P_{BL} in the power on stage and 20 seconds later it will return to typical value. Thus, the power source capacity for inverter should be considered to supply the initial power consumption at power on duration.

3.2.3 INVERTER INTERTFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal/External PWM Select Voltage	HI	V_{SEL}	—	2.0	—	5.0	V	
	LO		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	V_{SEL} = L	—	—	3.0	V	minimum duty ratio
	MIN			—	0	—	V	maximum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	V_{SEL} = H	2.0	—	5.0	V	duty on
	LO			0	—	0.8	V	duty fff
Control Signal Rising Time		T_r	—	—	—	100	ms	
Control Signal Falling Time		T_f	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	MΩ	
BLON Delay Time		T_{on}	—	500	—	—	ms	
BLON Off Time		T_{off}	—	500	—	—	ms	

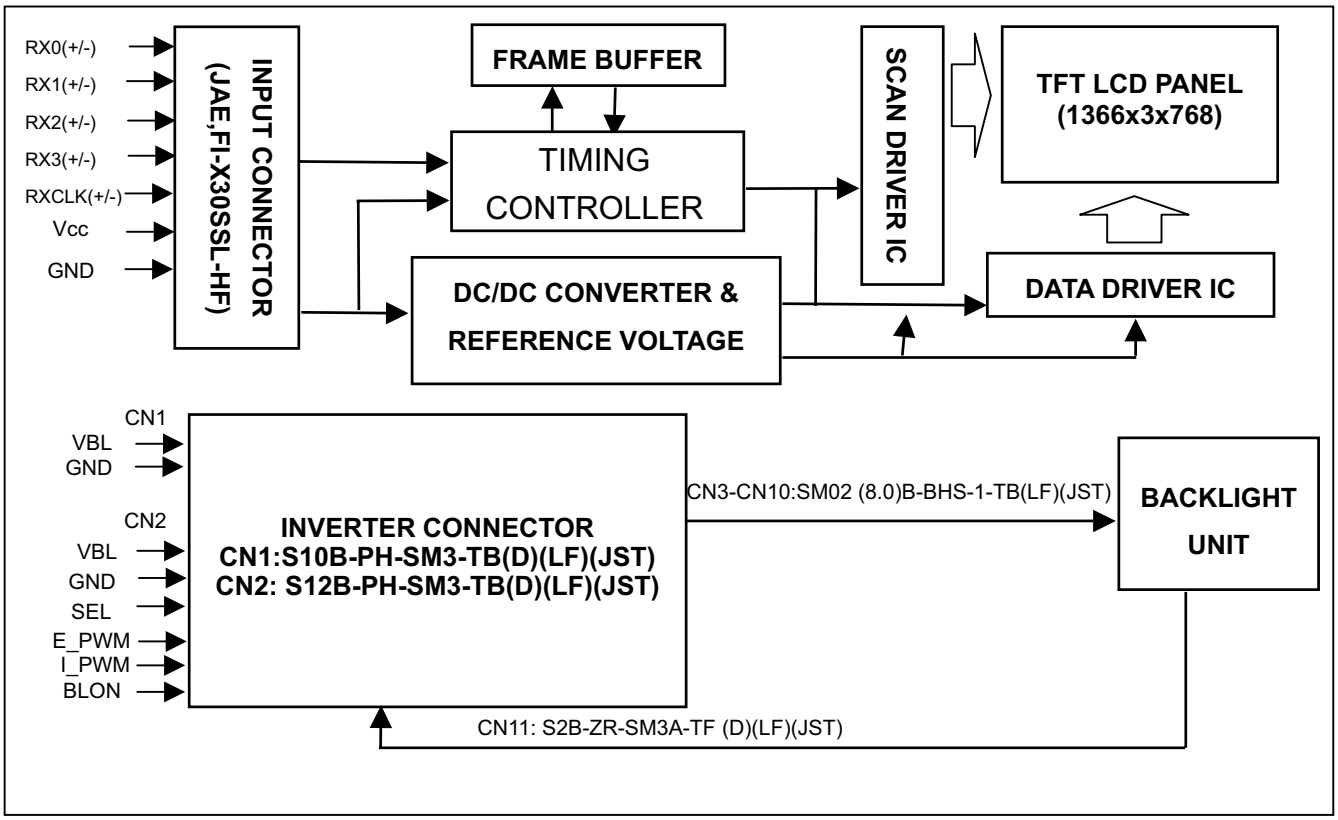
Note (1) The SEL signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM selection (SEL) during backlight turn on period.

Note (2) The power sequence and control signal timing are shown as the following figure.


VBL
0
Ton
Toff
VBLON
2.0V
0.8V
0
Backlight on duration
Tr
Tf
VSEL
2.0V
0.8V
0
Int. Dimming Function
Ext. Dimming Function
TPWMR
TPWMF
VEPWM
2.0V
0.8V
0
3.0V
VIPWM
0
VW
External PWM Period
External PWM Duty
Minimun Duty
100%

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	GND	Ground	
2	RPF	Display Rotation	(3)
3	SELLVDS	Select LVDS data format	(5)
4	NC	No Connection	(2)
5	NC	No Connection	
6	ODSEL1	Overdrive Lookup Table Selection	(4)
7	ODSEL2	Overdrive Lookup Table Selection	
8	GND	Ground	
9	RX0-	Negative transmission data of pixel 0	
10	RX0+	Positive transmission data of pixel 0	
11	RX1-	Negative transmission data of pixel 1	
12	RX1+	Positive transmission data of pixel 1	
13	RX2-	Negative transmission data of pixel 2	
14	RX2+	Positive transmission data of pixel 2	
15	RXCLK-	Negative of clock	
16	RXCLK+	Positive of clock	
17	RX3-	Negative transmission data of pixel 3	
18	RX3+	Positive transmission data of pixel 3	
19	GND	Ground	
20	GND	Ground	
21	GND	Ground	
22	GND	Ground	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	
26	VCC	Power supply: +5V	
27	VCC	Power supply: +5V	
28	VCC	Power supply: +5V	
29	VCC	Power supply: +5V	
30	VCC	Power supply: +5V	

Note (1) Connector Part No.: FI-X30SSL-HF(JAE) or compatible

Note (2) Reserved for internal use. Left it open.

Note (3) Low : normal display (default), High : display with 180 degree rotation

Note (4) Overdrive lookup table selection. The Overdrive lookup table should be selected in accordance to the frame rate to optimize image quality.

ODSEL2	ODSEL1	Note
L	L	Lookup table was optimized for 60 Hz frame rate.
L	H	Lookup table was optimized for 50 Hz frame rate.
H	L	Reserved. Do not use.
H	H	Reserved. Do not use.

Note (5) Please refer to 5.5 LVDS INTERFACE (Page 17)

5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN3-CN10 (Housing): BHR-03VS-1(JST)

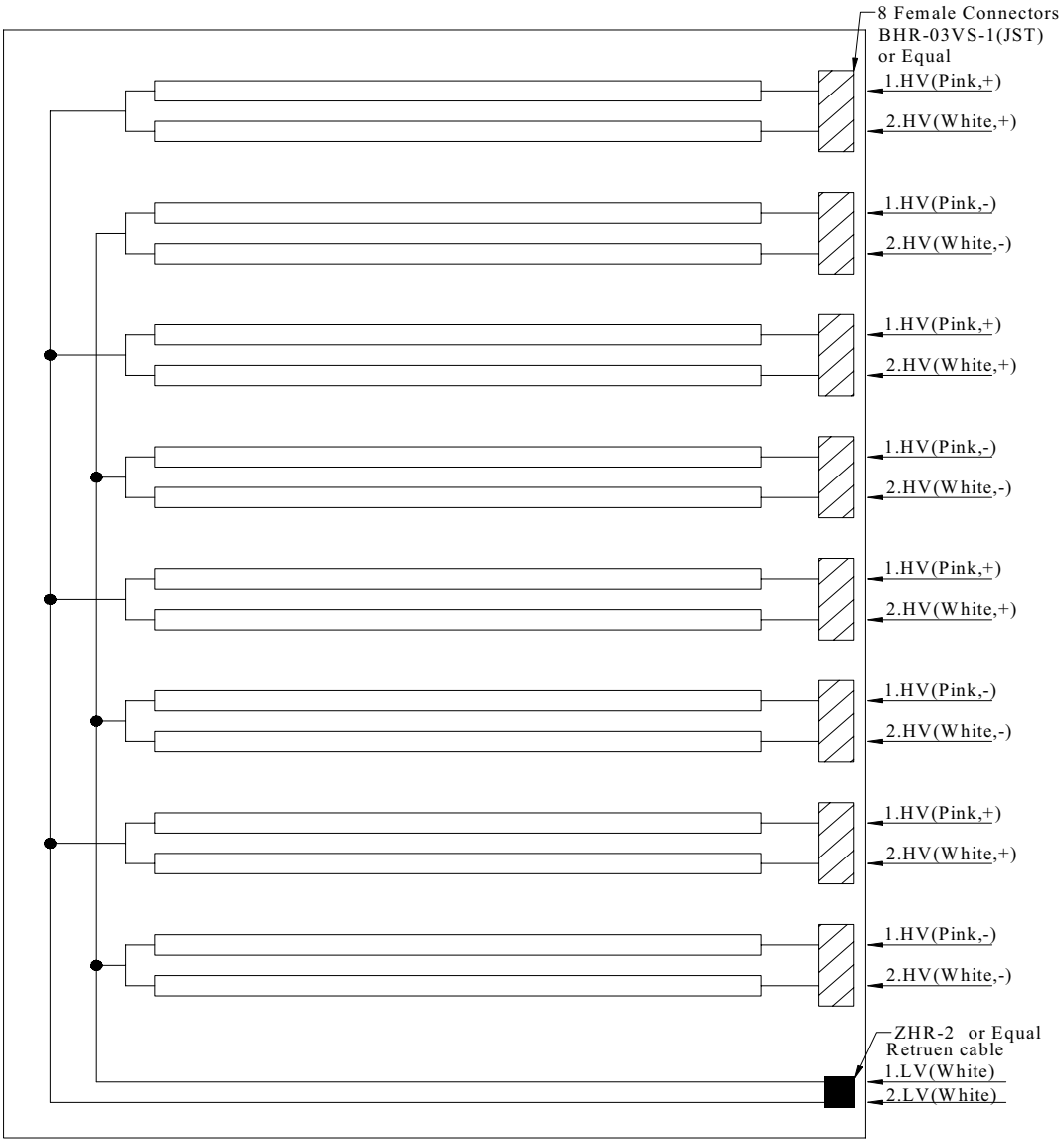
Pin No.	Symbol	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-03VS-1, manufactured by JST. The mating header on inverter part number is SM02(8.0)B-BHS-1-TB(LF).

CN11 (Housing): ZHR-2 (JST)or equivalent

Pin No.	Symbol	Description	Wire Color
1	LV	Low Voltage (+)	Black
2	LV	Low Voltage (-)	White

Note (2) The backlight interface housing and return cable for low voltage side is a model ZHR-2 , manufactured by JST or equivalent. The mating header on inverter part number is S2B-ZR-SM3A-TF(D)(LF) or equivalent.



5.3 INVERTER UNIT

CN1(Header):S10B-PH-SM3-TB(D)(LF)(JST) or equivalent.

Pin No.	Symbol	Description
1	VBL	+24V Power input
2		
3		
4		
5		
6	GND	Ground
7		
8		
9		
10		

CN2(Header): S12B-PH-SM3-TB(D)(LF)(JST) or equivalent..

Pin No.	Symbol	Description
1	VBL	+24V Power input
2		
3		
4		
5	NC	NC
6	GND	Ground
7		
8		
9	SEL	Internal/external PWM selection High : external dimming Low : internal dimming
10	E_PWM	External PWM control signal E_PWM should be connected to low when internal PWM was selected (SEL = low).
11	I_PWM	Internal PWM control signal I_PWM should be connected to ground when external PWM was selected (SEL = high).
12	BLON	Backlight on/off control

CN3-CN10(Header): SM02(8.0)B-BHS-1-TB(LF)(JST)

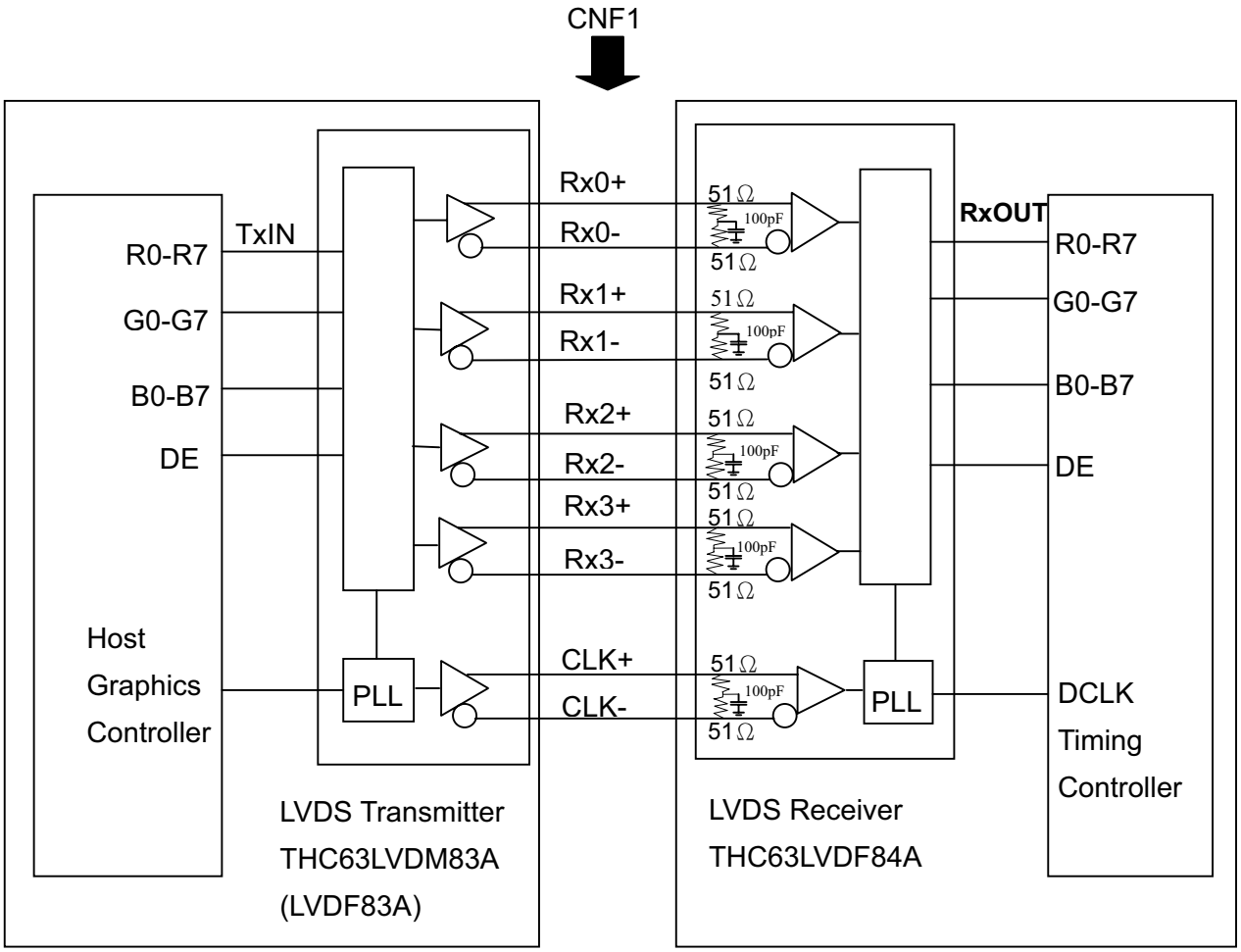
Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

CN11(Header): S2B-ZR-SM3A-TF(D)(LF)(JST) or equivalent

Pin No.	Symbol	Description
1	CCFL COLD	CCFL low voltage (+)
2	CCFL COLD	CCFL low voltage (-)

Note (1) Floating of any control signal is not allowed.

5.4 BLOCK DIAGRAM OF INTERFACE



R0~R7 : Pixel R Data ,
G0~G7 : Pixel G Data ,
B0~B7 : Pixel B Data ,
DE : Data enable signal

Note (1) The system must have the transmitter to drive the module.
Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.5 LVDS INTERFACE

	SIGNAL		TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT	
	SELLVDS =L	SELLVDS =H	PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	SELLVDS =L	SELLVDS =H
	R0	R2	51	TxIN0			27	Rx OUT0	R0	R2
	R1	R3	52	TxIN1			29	Rx OUT1	R1	R3
	R2	R4	54	TxIN2	TA OUT0+	Rx 0+	30	Rx OUT2	R2	R4
	R3	R5	55	TxIN3			32	Rx OUT3	R3	R5
	R4	R6	56	TxIN4			33	Rx OUT4	R4	R6
	R5	R7	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5	R7
	G0	G2	4	TxIN7			37	Rx OUT7	G0	G2
	G1	G3	6	TxIN8			38	Rx OUT8	G1	G3
	G2	G4	7	TxIN9			39	Rx OUT9	G2	G4
	G3	G5	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3	G5
	G4	G6	12	TxIN13			45	Rx OUT13	G4	G6
	G5	G7	14	TxIN14			46	Rx OUT14	G5	G7
	B0	B2	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0	B2
	B1	B3	19	TxIN18			51	Rx OUT18	B1	B3
24	B2	B4	20	TxIN19			53	Rx OUT19	B2	B4
bit	B3	B5	22	TxIN20			54	Rx OUT20	B3	B5
	B4	B6	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4	B6
	B5	B7	24	TxIN22			1	Rx OUT22	B5	B7
	DE	DE	30	TxIN26			6	Rx OUT26	DE	DE
	R6	R0	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6	R0
	R7	R1	2	TxIN5			34	Rx OUT5	R7	R1
	G6	G0	8	TxIN10			41	Rx OUT10	G6	G0
	G7	G1	10	TxIN11			42	Rx OUT11	G7	G1
	B6	B0	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6	B0
	B7	B1	18	TxIN17			50	Rx OUT17	B7	B1
	RSVD 1	RSVD 1	25	TxIN23			2	Rx OUT23	NC	NC
	RSVD 2	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	NC	NC
	RSVD 3	RSVD 3	28	TxIN25			5	Rx OUT25	NC	NC
		DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK	

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE: Data enable signal

Notes(1) RSVD(reserved)pins on the transmitter shall be “H” or “L”.

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

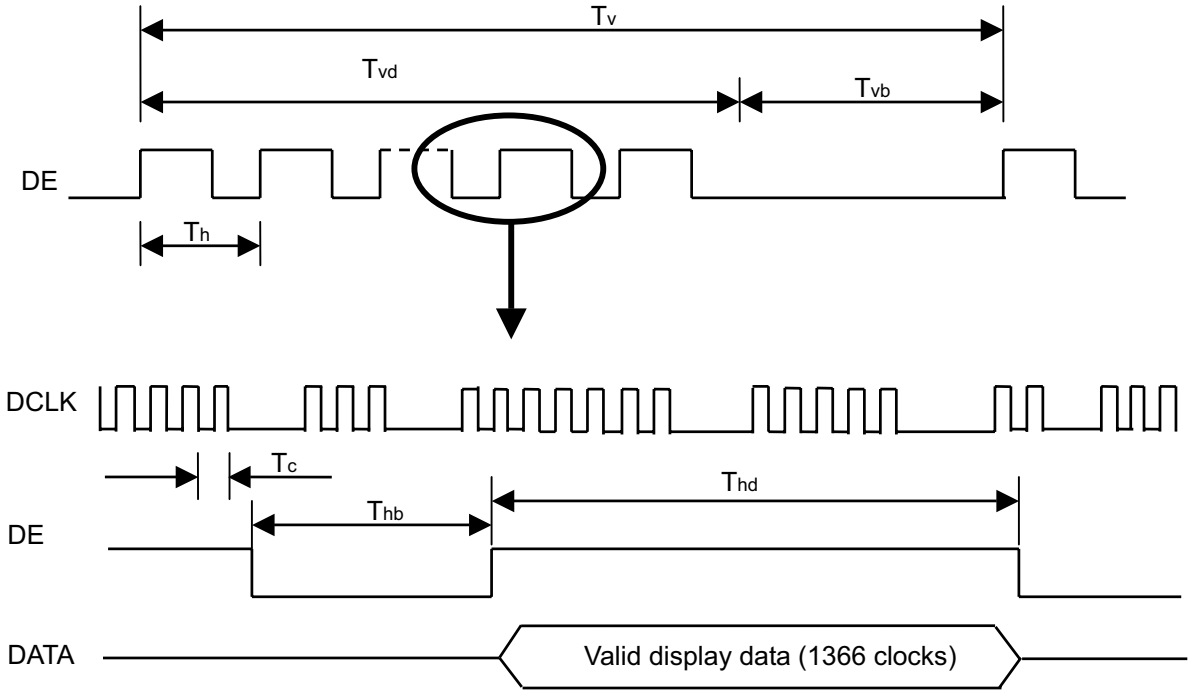
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	86	88	MHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr5	47	50	53	Hz	(2)
		Fr6	57	60	63	Hz	(3)
	Total	Tv	778	795	888	Th	Tv=Tvd+Tvb
	Display	Tvd	768	768	768	Th	-
	Blank	Tvb	10	27	120	Th	-
Horizontal Active Display Term	Total	Th	1436	1798	1936	Tc	Th=Thd+Thb
	Display	Thd	1366	1366	1366	Tc	-
	Blank	Thb	70	432	570	Tc	-

Note (1) Since this module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

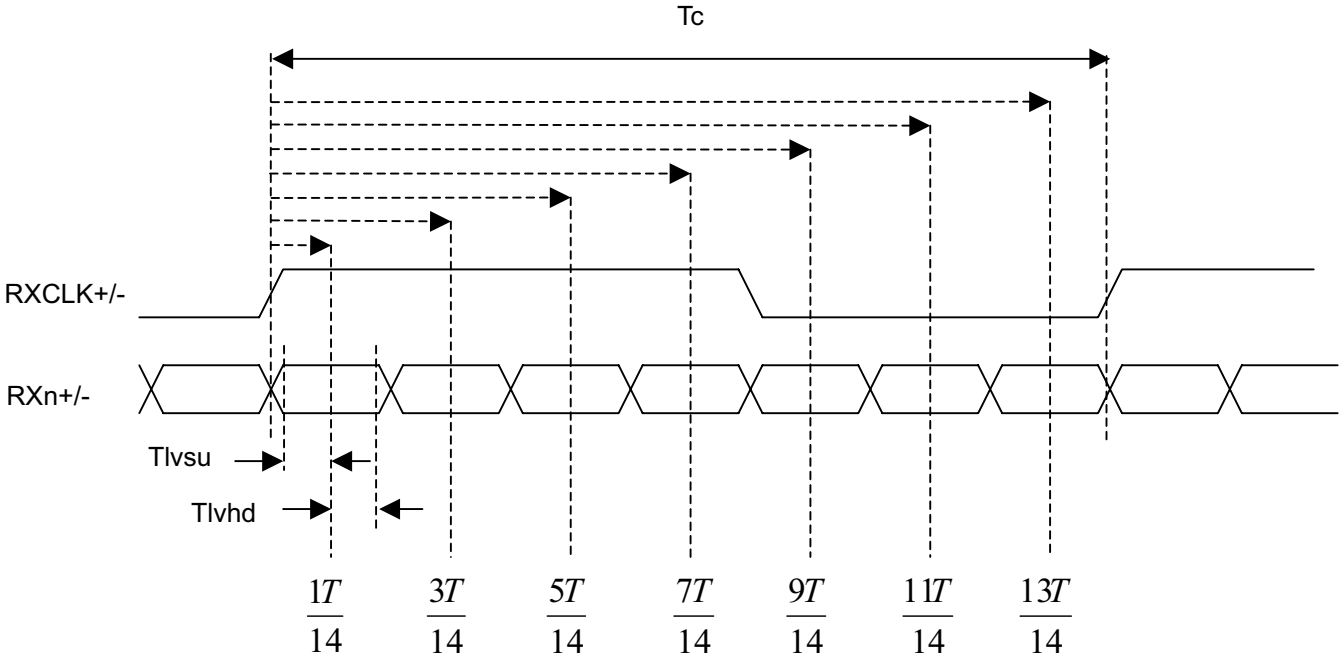
(2) (ODSEL2, ODSEL1) = (L,H). Please refer to 5.1 for detail information.

(3) (ODSEL2, ODSEL1) = (L,L). Please refer to 5.1 for detail information.

INPUT SIGNAL TIMING DIAGRAM

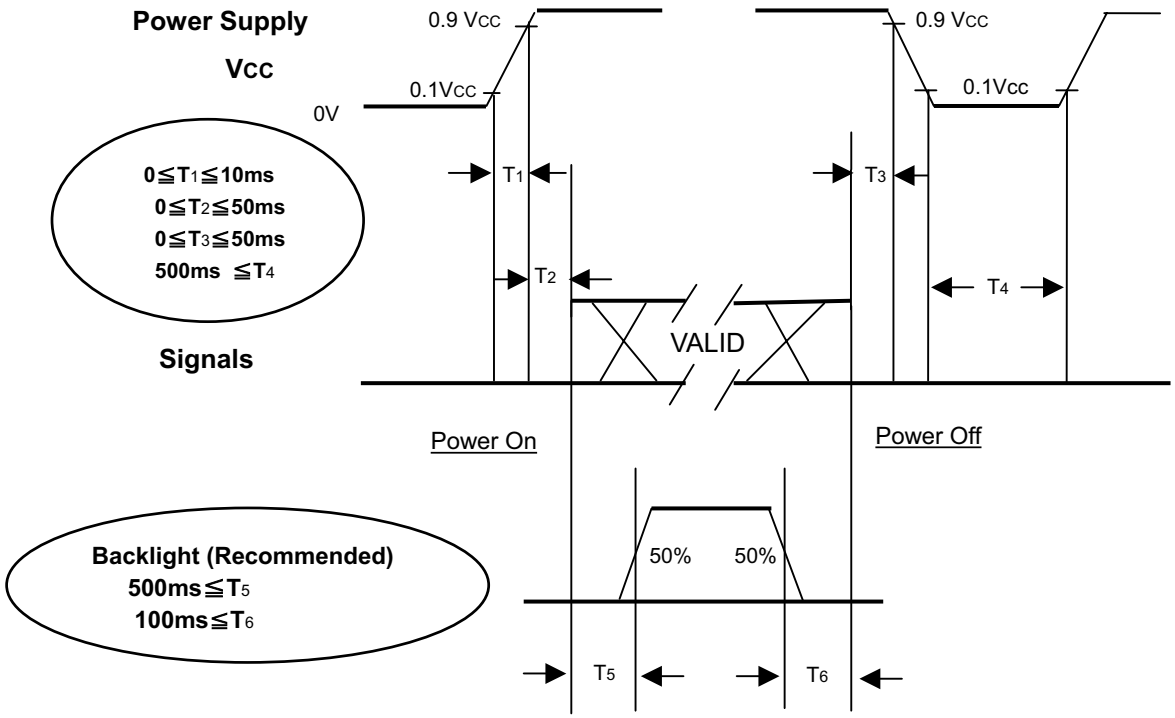


LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	4.5 ± 0.5	mA
Oscillating Frequency (Inverter)	F_W	62.5 ± 3	KHz

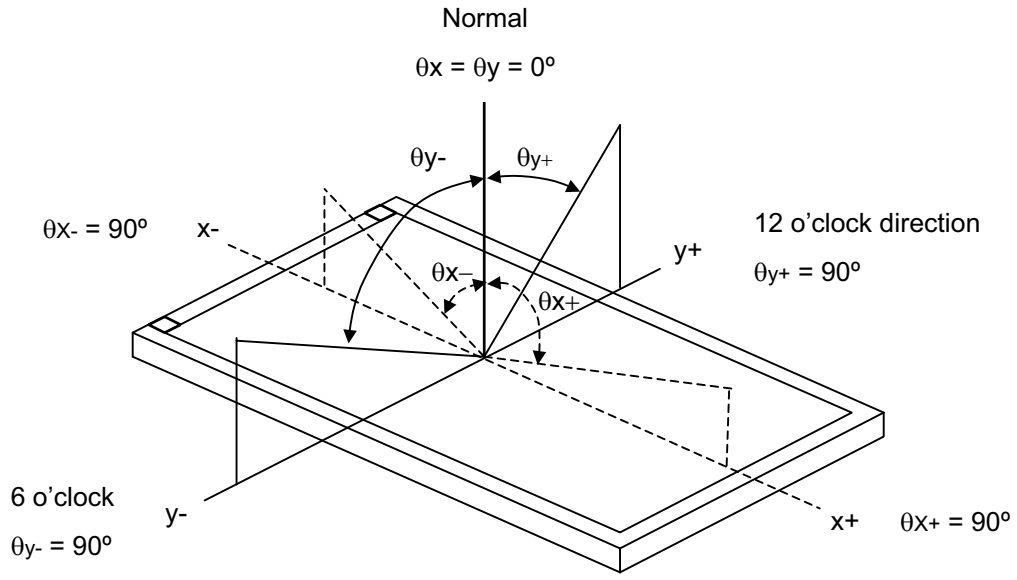
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	800	1000	-	-	(2)
Response Time		Gray to gray average		-	8	12	ms	(3)
Center Luminance of White		L_C		450	550	-	cd/m^2	(4)
Average Luminance of White		L_{AVE}		400	450	-	cd/m^2	(4)
White Variation		δW		-	-	1.3	-	(7)
Cross Talk		CT		-	-	4.0	%	(5)
Color Chromaticity	Red	Rx		0.622	0.652	0.682	-	(6)
		Ry		0.302	0.332	0.362	-	
	Green	Gx		0.240	0.270	0.300	-	
		Gy		0.559	0.589	0.619	-	
	Blue	Bx		0.111	0.141	0.171	-	
		By		0.038	0.068	0.098	-	
	White	Wx		0.255	0.285	0.315	-	
		Wy		0.263	0.293	0.323	-	
	Color Gamut	CG		72	75		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88	-	Deg.	(1)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by EZ-Contrast 160R (Eldim)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

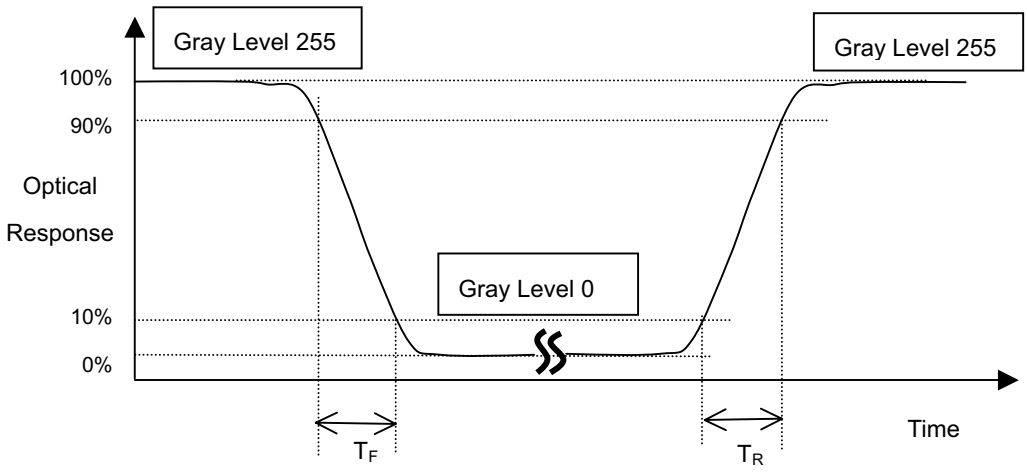
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

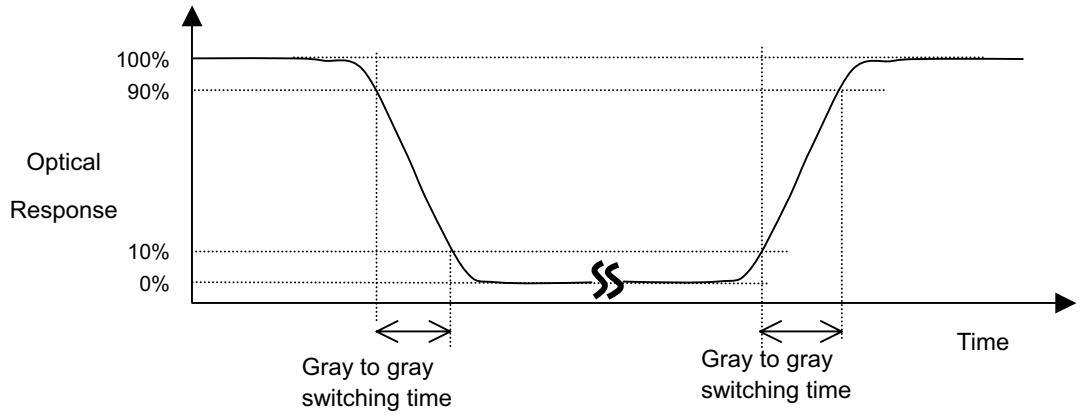
CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (8).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 63, 127, 191, 255.

Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each other .

Note (5) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$

$L_{AVE} = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

L (x) is corresponding to the luminance of the point X at the figure in Note (8).

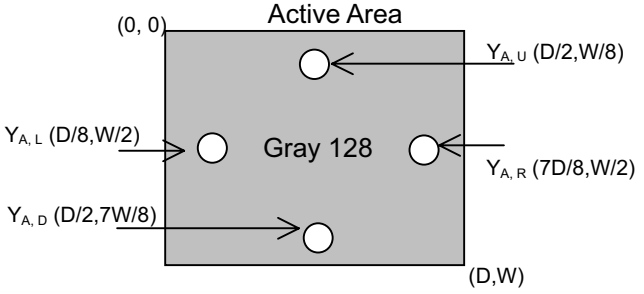
Note (6) Definition of Cross Talk (CT):

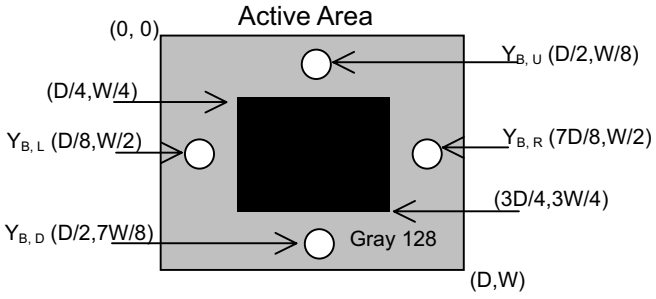
$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

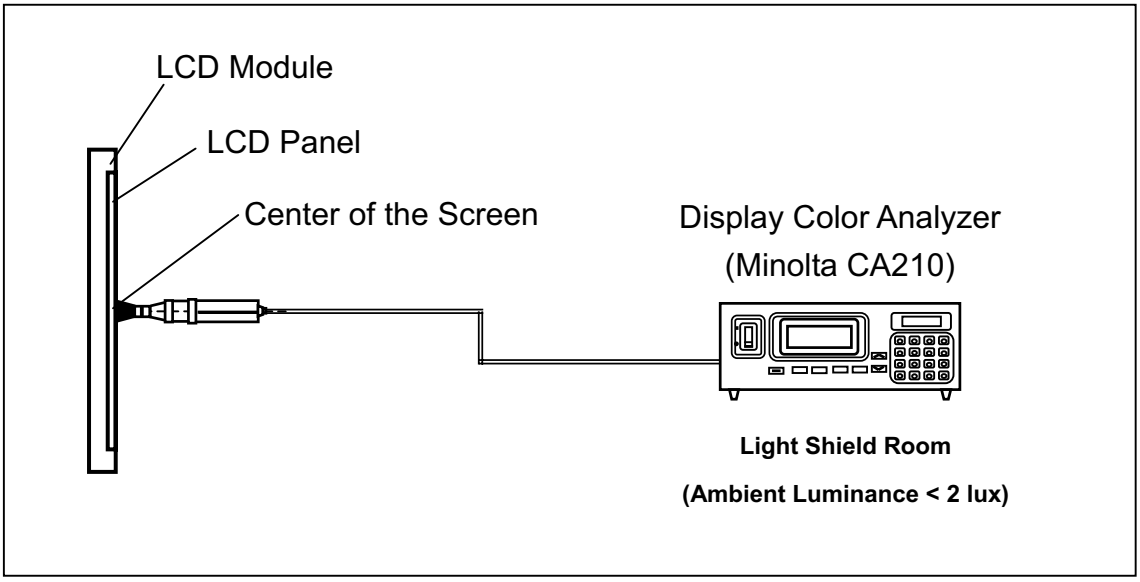
Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)





Note (7) Measurement Setup:

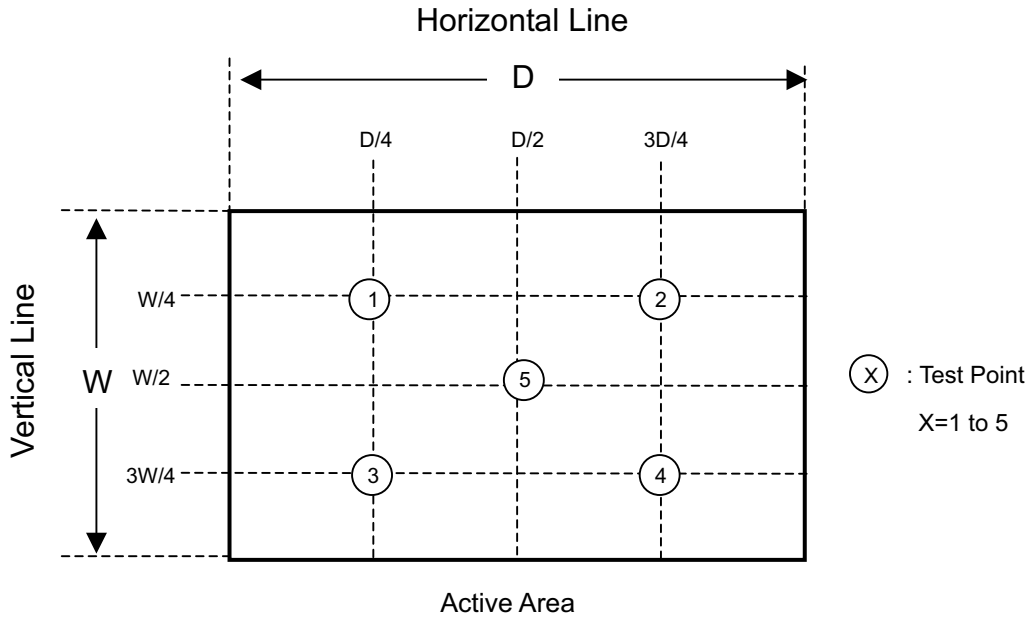
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



Note (8) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

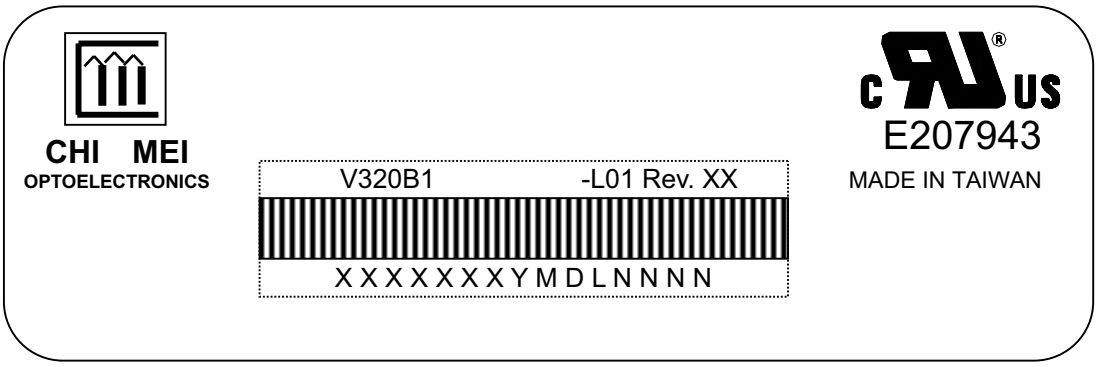
δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

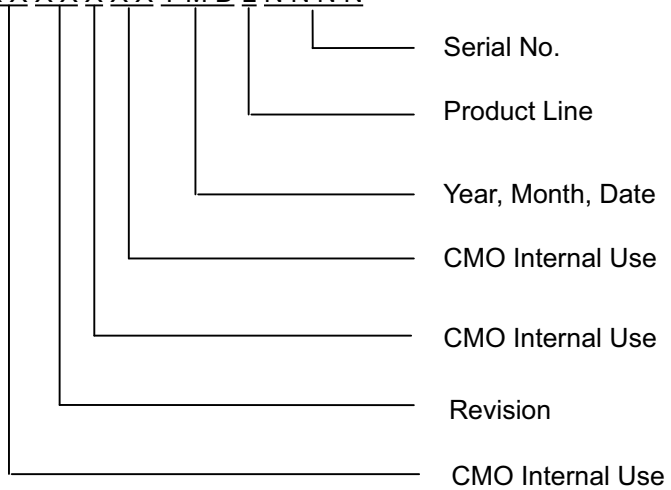
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V320B1-L01

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 4 LCD TV modules / 1 Box

(2) Box dimensions : 906(L) X 384 (W) X 580 (H)

(3) Weight : approximately 28Kg (4 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

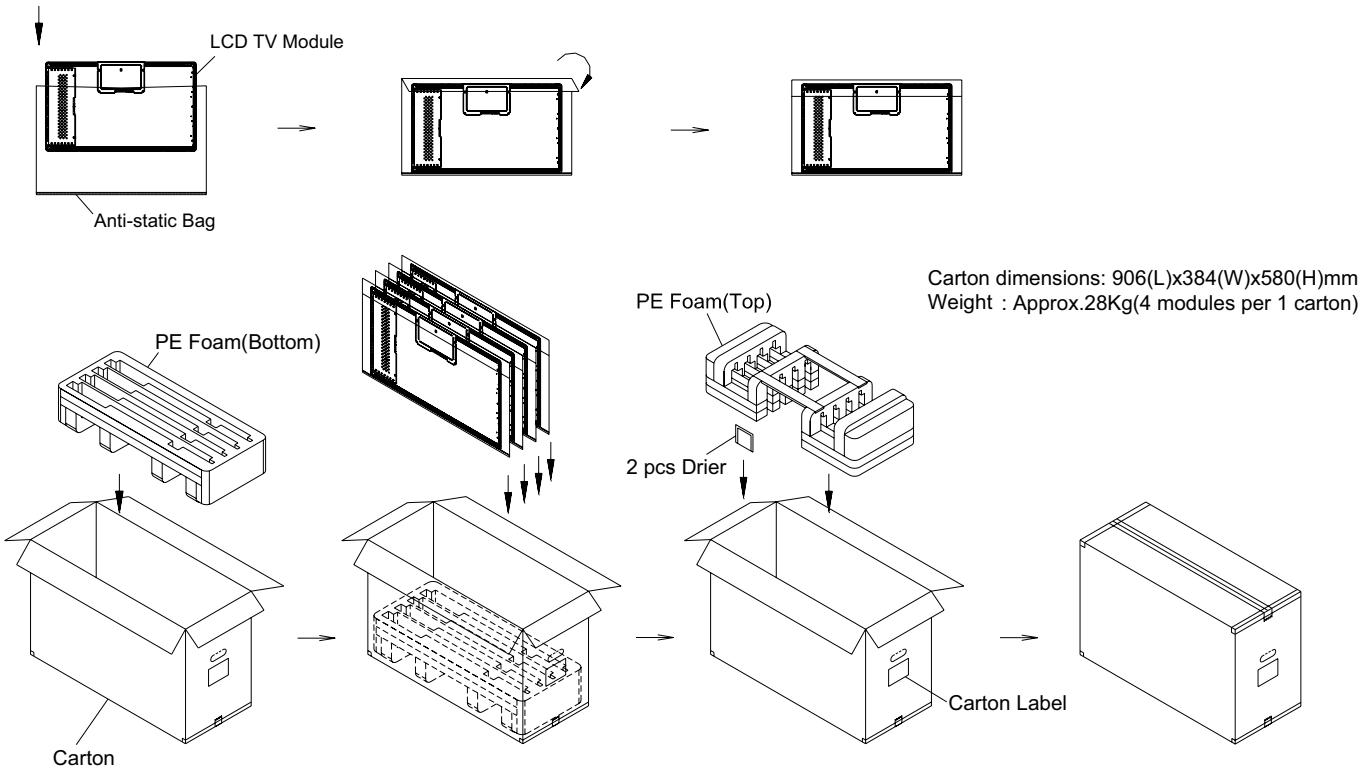


Figure.9-1 packing method

Corner Protector:L1130*50mm*50mm
Pallet:L1000*W1180*H145mm
Bottom Cap:L1000*W1180*H120mm
Pallet Stack:L1000*W1180*H1305mm
Gross:188kg

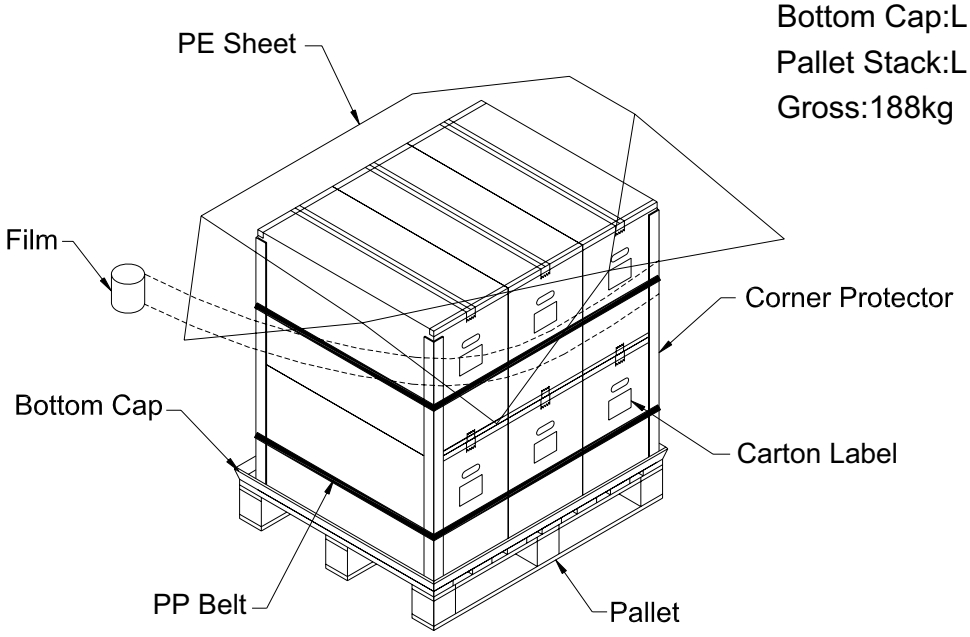


Figure. 9-2 Packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

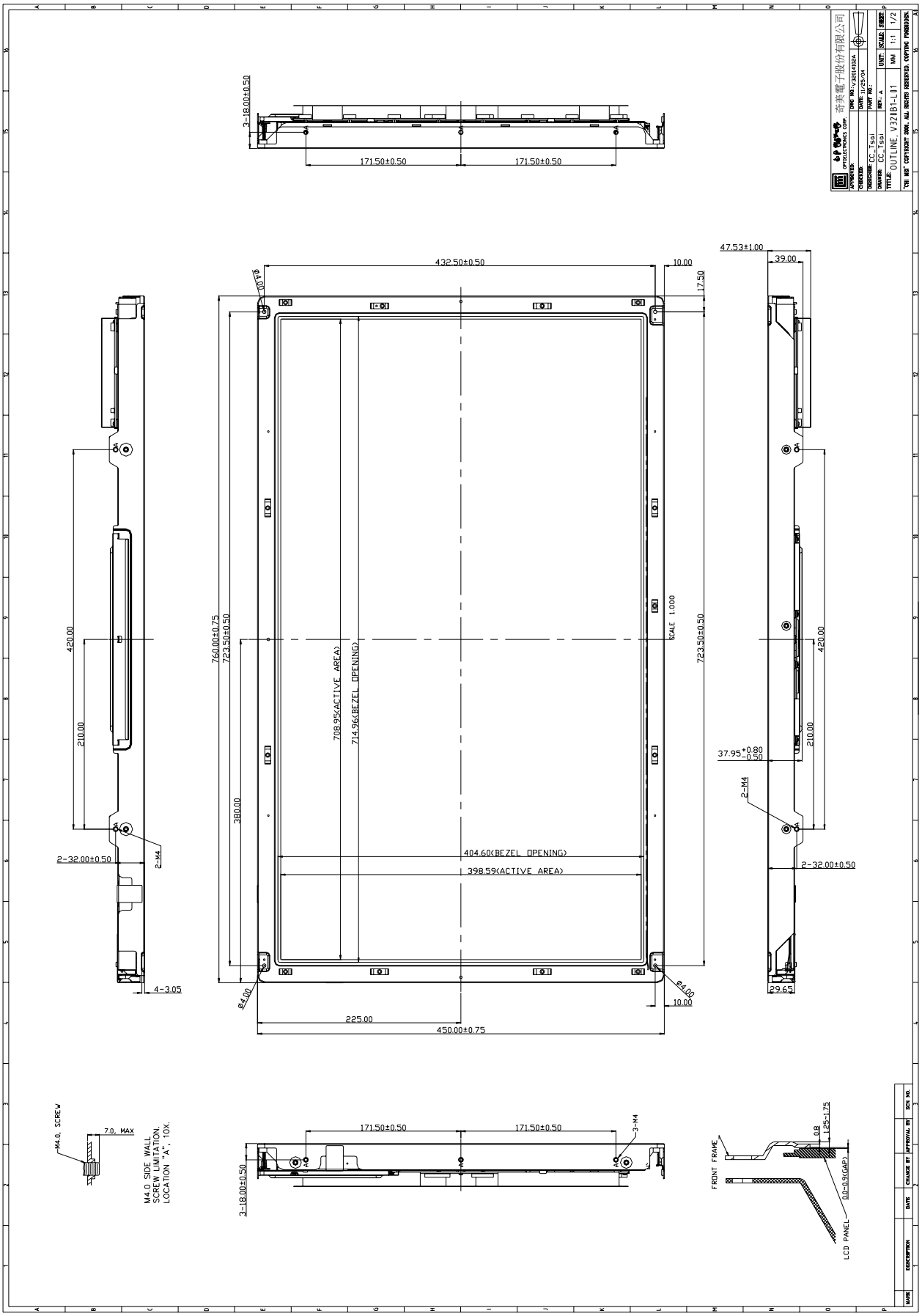
10.2 SAFETY PRECAUTIONS

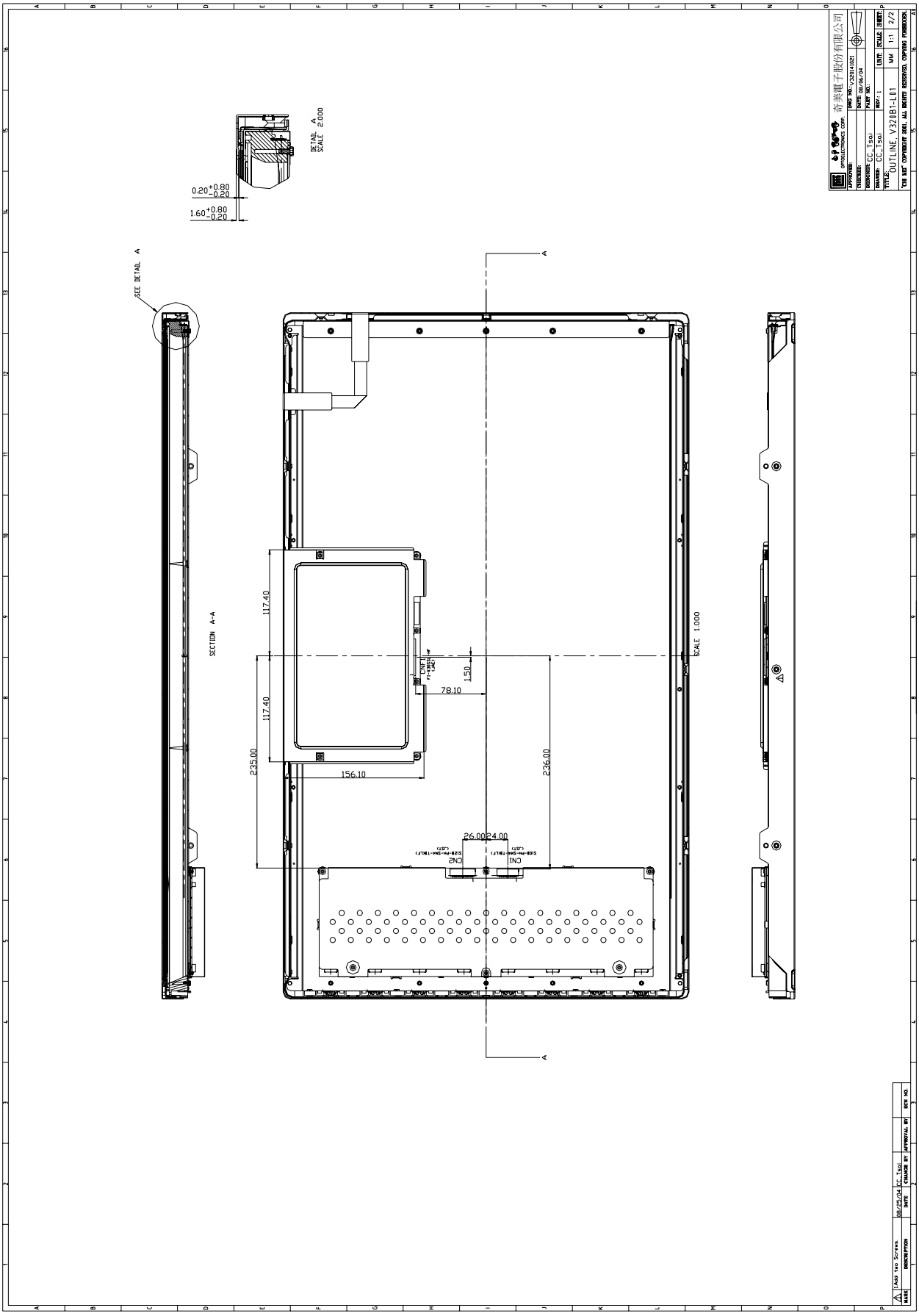
(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

11. MECHANICAL CHARACTERISTICS




DETAIL A
SCALE 2.000
0.20 +0.80 -0.20
1.60 +0.80 -0.20
SEE DETAIL A
SECTION A-A
SCALE 1.000
117.40
117.40
235.00
156.10
78.10
1.50
236.00
26.00
24.00
CN2
CN1
OUTLINE, V320B1-L01

Basic Operations & Circuit Description

Main Electric Components

(1). MODULE:

There are 1 pc. panel and 2 pcs. PCB including 1 pc. INVERTER board(L), 1 pc. T-CONTROL board,

(2).SIGNAL PROCESS

There are 4 pcs. PCBs including

1 pc. Audio&Tuner board,
1 pc. Main digital board,
1 pc. Keypad board,
1 pc. Remote Control Receiver board,

(3).POWER

There are 1 pc. PCB for power.

PCB function

1. Power:

(1). Input voltage: AC 100V~240V, 47Hz~63Hz.
Input range: AC 90V(Min)~264V(Max) auto regulation.
(2). To provide power for PCBs.
a). +24V for Inverter.
b). +5Vsb for standby,
c). +5V for signal power,
d). +24V for Audio Amp power and converter to
e). +12V for Tuner power.

2. Main (Video InterFace) board:

(1).Decoder the video signal (TV,CVBS,S-VIDEO) from analog to digital signal.
(2).Converter the Video signals(TV,CVBS,S-VIDEO) and graphics signal (VGA,YPbPr) from internace to progressive,
(3). Converter the Digital to fit the panel display mode and output the LVDS signal to Panel.

3. Tuner & Audio Board：

(1)Convert TV RF signal to video and audio signal to Main board.
(2). Decoder the TV SIF signal to audio signal,
(3). Converter the audio to audio Ampifile and out put to the speaker.

4. KEYBOARD

To get the main button control on LCD_TV as SOURCE,MENU, CHANEL +,CHANEL -, VOL +,VOL-, STANDBY functions.

5. Remote control board

Receive the remote signal and active for the control.

6. T-CONTROL board

Converter the LVDS signal to the digital signal for fitting the PANEL.

7. INVERTER board

Converter the low DC voltage +24V to high AC voltage to drive the backlight.

PCB failure analysis

1. CONTROL:

a. Abnormal noise on screen.

b. No picture.

2. MAIN (VIDEO):

a. Lacking color, Bad color scale.

b. No voice.

c. No picture but with signals output, OSD and back light.

d. Abnormal noise on screen.

3. POWER:

No picture, no power output.

Basic operation of LCD-TV

1. After turning on power switch, power board sends 5Vst-by Volt to Micro Processor IC waiting for ON signals from Key Switch or Remote Receiver.

2. When the ON signal from Key Switch or Remote Receiver is detected, Micro Processor will send ON Control signals to Power. Then Power sends (5Vsc, 12Vsc, 24V and RLY ON, Vs ON) to PCBs working. This time VIF will send signals to display back light, OSD on the panel and start to search available signal sources. If the audio signals input, them will be amplified by Audio AMP and transmitted to Speakers.

3. If some abnormal signals are detected (for example: over volts, over current, over temperature and under volts), the system will be shut down by Power off.

LCD basic display theory.

When an electrical field is applied to the LC planes, the LC molecules re-align themselves so that they are parallel to the electrical field. This electrical process is known as **twisted nematic field effect** or **TNFE**. In this alignment, polarized light is not twisted as it passes through the LC material (see Diagram 3A and 3B). If the front polarizer is oriented perpendicular to the rear polarizer, light will pass through the energized display but will be blocked by the rear polarizer. An LCD in this form is acting as a light shutter.

Displays with variable characters are created by selectively etching away the conductive surface that was originally deposited on the glass. Etched areas become the display's background; unetched areas become the display's characters.

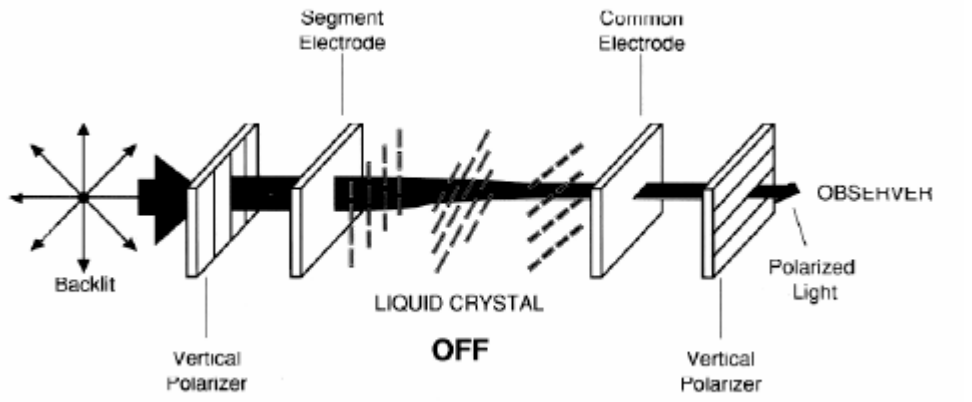


Diagram 3A. The "off" state of a TN LCD-the LC molecules form a twist and therefore cause polarized light to twist as it passes through.

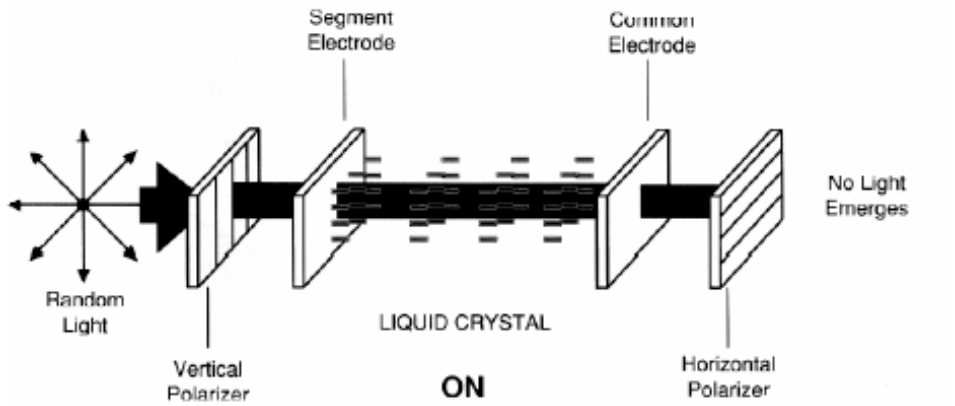
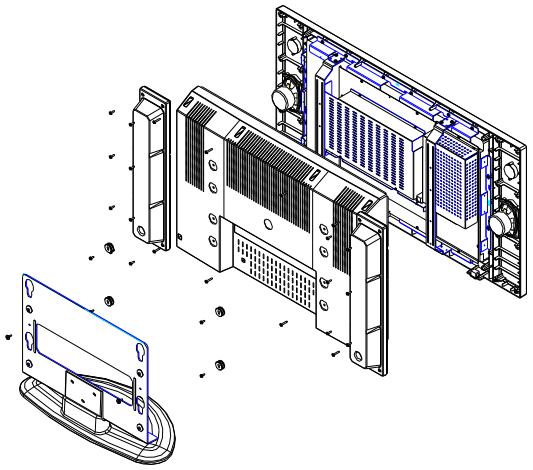


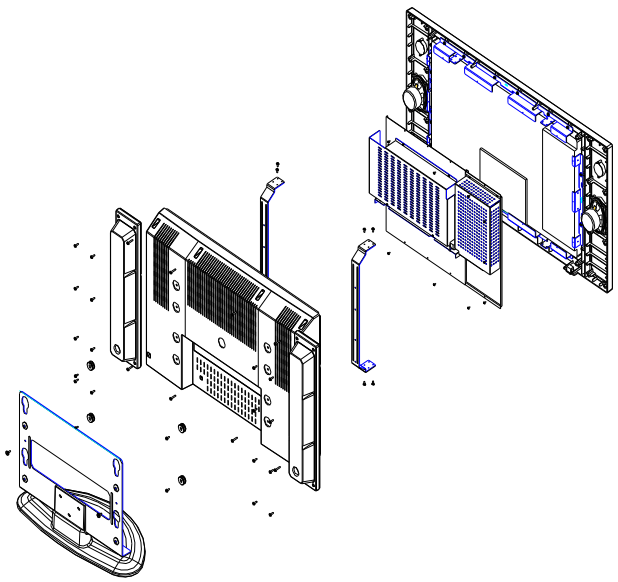
Diagram 3B. The "on" state-the electrical field re-aligns the LC molecules so they do not twist the polarized light.

Disassembly

In case of trouble, etc., Necessitating disassemble, please disassemble in the order shown in the illustrations.
Reassemble in the reverse order.
1. Removal of the Back Cover



2. Removal of the MAIN PCB
   a. Remove the screws.
   b · Slide out the LCD chassis slightly; pull up the connector of AC cord from PCB; pull up the LCD PCB from LCD.
   c . Remove the Anode cap from Thepicture tube. To avaid a shock hazard, be sure to discharge
   d · Take out the LCD chassis.



IC DESCRIPTION

-MT8205G

-AT24C02

-MX29LV160BBTC

-LP2996

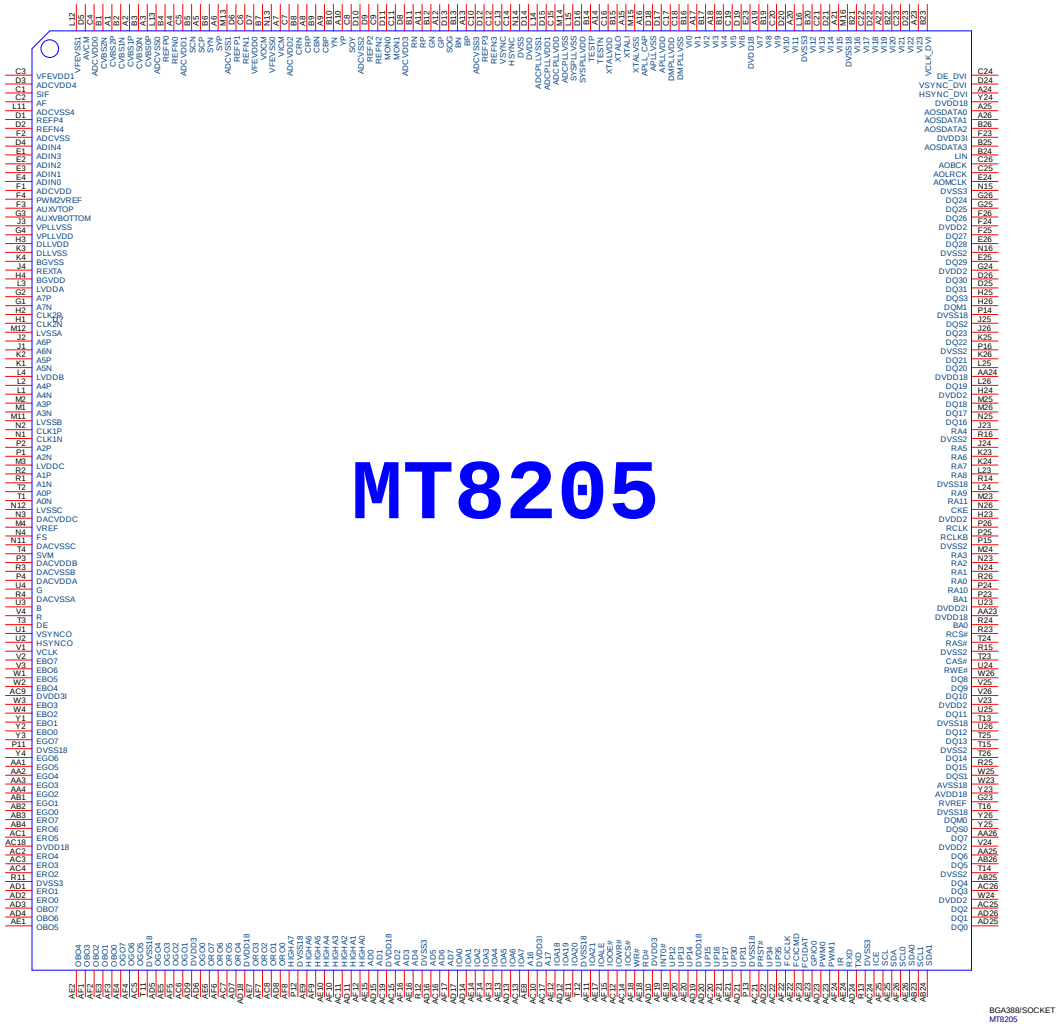
-AZ1117/H

-WM8776

-MX232A

-ISAV330

Pinout information



2.3 Pin Descriptions

Table 2-1 provides detail video/audio port pin descriptions.

Table 2-1 video/audio port pin descriptions.

Pin	Symbol	Type	Description
E24	AOMCLK	O	Audio out master clock
C25	AOLRCK	O	Audio out left-right clock
C26	AOBCK	O	Audio out bit clock
A25	AOSDATA0	O	Audio out data line 0
A26	AOSDATA1	O	Audio out data line 1
B26	AOSDATA2	O	Audio out data line 2
B25	AOSDATA3	O	Audio out data line 3
B24	LIN	I	Audio line in
A3	CVBS0P	I	Composite Video input 0
A2	CVBS1P	I	Composite Video input 1
A1	CVBS2P	I	Composite Video input 2
C1	SIF	I	Tuner Sound SIF
C2	AF	I	Tuner Sound AF

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
  - **2.5 (V_{CC} = 2.5V to 5.5V)**
  - **1.8 (V_{CC} = 1.8V to 5.5V)**
- **Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)**
- **2-Wire Serial Interface**
- **Bidirectional Data Transfer Protocol**
- **100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **8-Byte Page (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes**
- **Partial Page Writes Are Allowed**
- **Self-Timed Write Cycle (10 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Cycles**
  - **Data Retention: 100 Years**
- **Automotive Grade and Extended Temperature Devices Available**
- **8-Pin and 14-Pin JEDEC SOIC and 8-Pin PDIP Packages**

Description

The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C01A/02/04/08/16 is available in space saving 8-pin PDIP, 8-pin and 14-pin SOIC packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

2-Wire Serial CMOS E^2PROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

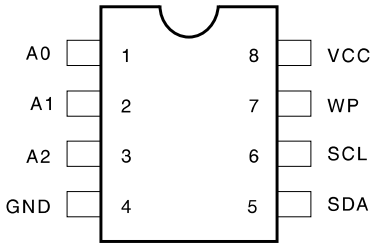
8K (1024 x 8)

16K (2048 x 8)

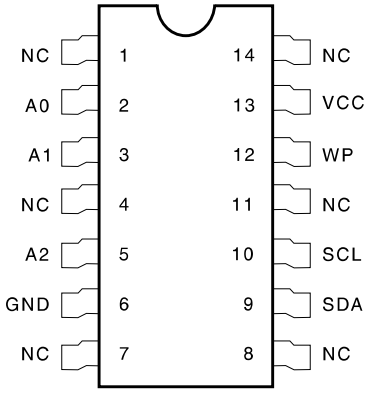
Pin Configurations

Pin Name	Function
A_0 to A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

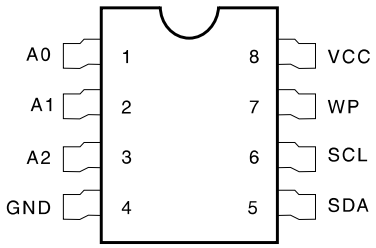
8-Pin PDIP



14-Pin SOIC



8-Pin SOIC



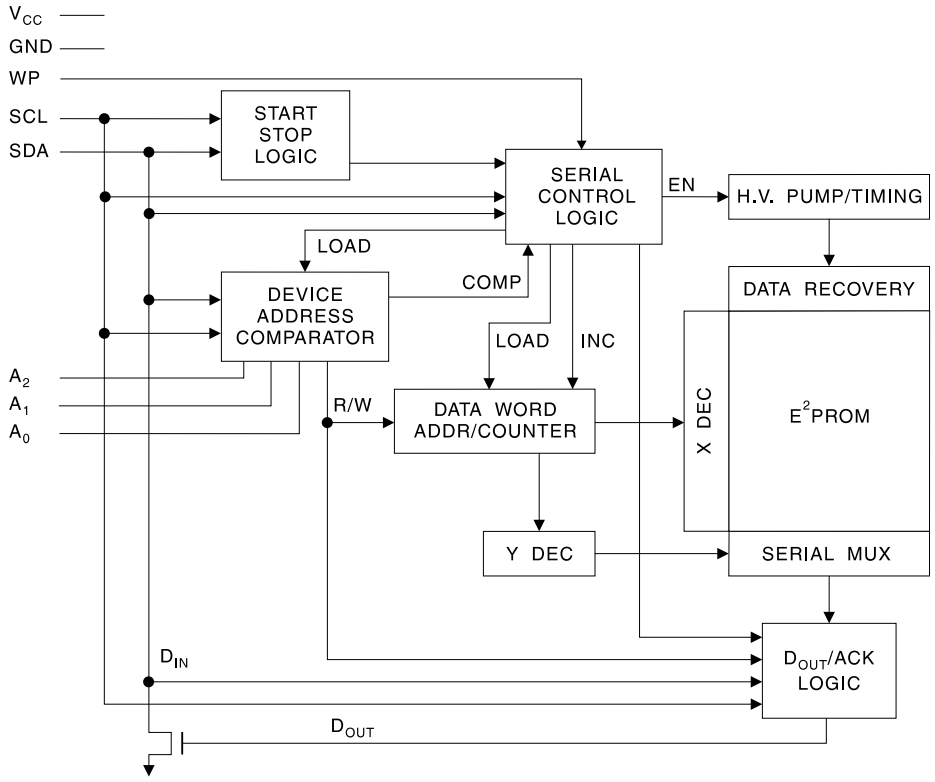
0180C

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each E^2PROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16 does not use the device address pins which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

(continued)

MX29LV160BT/BB

16M-BIT [2Mx8/1Mx16] CMOS SINGLE VOLTAGE 3V ONLY FLASH MEMORY

FEATURES

- Extended single - supply voltage range 2.7V to 3.6V
- 2,097,152 x 8/1,048,576 x 16 switchable
- Single power supply operation
  - 3.0V only operation for read, erase and program operation
- **Fully compatible with MX29LV160A device**
- Fast access time: 70/90ns
- Low power consumption
  - 30mA maximum active current
  - 0.2uA typical standby current
- Command register architecture
  - Byte/word Programming (9us/11us typical)
  - Sector Erase (Sector structure 16K-Bytex1, 8K-Bytex2, 32K-Bytex1, and 64K-Byte x31)
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors with Erase Suspend capability.
  - Automatically program and verify data at specified address
- Erase Suspend/Erase Resume
  - Suspends sector erase operation to read data from, or program data to, any sector that is not being erased, then resumes the erase.
- Status Reply
  - Data polling & Toggle bit for detection of program and erase operation completion.
- Ready/Busy pin (RY/BY)
  - Provides a hardware method of detecting program or erase operation completion.
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Temporary sector unprotect allows code changes in previously locked sectors.
- CFI (Common Flash Interface) compliant
  - Flash device parameters stored on the device and provide the host system to access
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Boot Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Low VCC write inhibit is equal to or less than 1.4V
- Package type:
  - 44-pin SOP
  - 48-pin TSOP
  - 48-ball CSP
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash
- 10 years data retention

GENERAL DESCRIPTION

The MX29LV160BT/BB is a 16-mega bit Flash memory organized as 2M bytes of 8 bits or 1M words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LV160BT/BB is packaged in 44-pin SOP, 48-pin TSOP and 48-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29LV160BT/BB offers access time as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV160BT/BB has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29LV160BT/BB uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling. The MX29LV160BT/BB uses a 2.7V~3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

November 2003

National Semiconductor

LP2996
DDR Termination Regulator

General Description

The LP2996 linear regulator is designed to meet the JEDEC SSTL-2 specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination. The LP2996 also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output as a reference for the chipset and DIMMs.

An additional feature found on the LP2996 is an active low shutdown ($\overline{SD}$) pin that provides Suspend To RAM (STR) functionality. When $\overline{SD}$ is pulled low the V_{TT} output will tri-state providing a high impedance output, but, V_{REF} will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

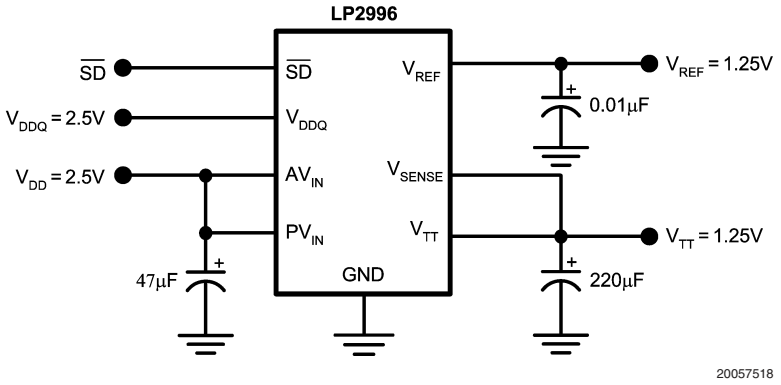
Features

- Source and sink current
- Low output voltage offset
- No external resistors required
- Linear topology
- Suspend to Ram (STR) functionality
- Low external component count
- Thermal Shutdown
- Available in SO-8, PSOP-8 or LLP-16 packages

Applications

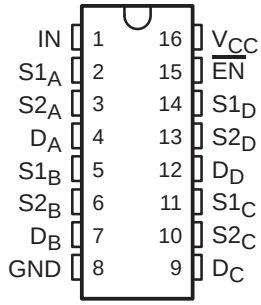
- DDR-I and DDR-II Termination Voltage
- SSTL-2 and SSTL-3 Termination
- HSTL Termination

Typical Application Circuit

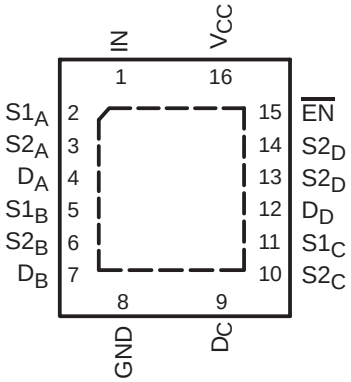


- **Low Differential Gain and Phase (D_G = 0.64%, D_P = 0.1 Degrees Typ)**
- **Wide Bandwidth (BW = 300 MHz Min)**
- **Low Crosstalk (X_{TALK} = −63 dB Typ)**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on} = 3 Ω Typ)**
- **V_{CC} Operating Range From 4.5 V to 5.5 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Data and Control Inputs Provide Undershoot Clamp Diode**
- **Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Suitable for Both RGB and Composite-Video Switching**

D, DBQ, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The TI TS5V330 video switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable ($\overline{EN}$) input. When $\overline{EN}$ is low, the switch is enabled and the D port is connected to the S port. When $\overline{EN}$ is high, the switch is disabled and the high-impedance state exists between the D and S ports. The select (IN) input controls the data path of the multiplexer/demultiplexer.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Tape and reel	TS5V330RGYR	TE330
	SOIC − D	Tube	TS5V330D	TS5V330
		Tape and reel	TS5V330DR	
	SSOP (QSOP) − DBQ	Tape and reel	TS5V330DBQR	TE330
	TSSOP − PW	Tube	TS5V330PW	TE330
		Tape and reel	TS5V330PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

wolfson microelectronics

WM8776

24-bit, 192kHz Stereo CODEC with 5 Channel I/P Multiplexer

DESCRIPTION

The WM8776 is a high performance, stereo audio CODEC with five channel input selector. The WM8776 is ideal for surround sound processing applications for home hi-fi, DVD-RW and other audio visual equipment.

A stereo 24-bit multi-bit sigma delta ADC is used with a five stereo channel input mixer. Each ADC channel has programmable gain control with automatic level control. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported.

A stereo 24-bit multi-bit sigma delta DAC is used with digital audio input word lengths from 16-32 bits and sampling rates from 32kHz to 192kHz. The DAC has an input mixer allowing an external analogue signal to be mixed with the DAC signal. There are also Headphone and line outputs, with volume controls for the headphones.

The WM8776 supports fully independent sample rates for the ADC and DAC. The audio data interface supports I^2S, left justified, right justified and DSP formats.

The device is controlled in software via a 2 or 3 wire serial interface, selected by the MODE pin, which provides access to all features including channel selection, volume controls, mutes, and de-emphasis facilities.

The device is available in a 48-pin TQFP package.

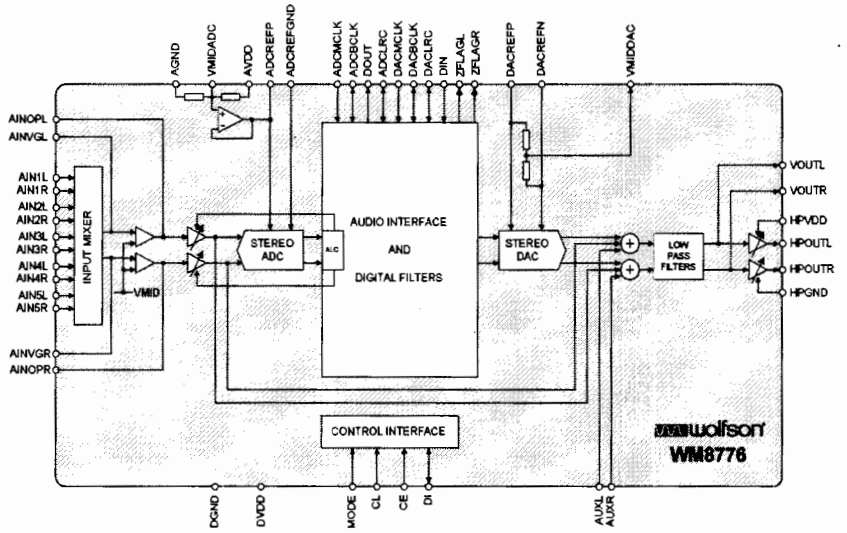
FEATURES

- Audio Performance
  - 108dB SNR ('A' weighted @ 48kHz) DAC
  - 102dB SNR ('A' weighted @ 48kHz) ADC
- DAC Sampling Frequency: 32kHz – 192kHz
- ADC Sampling Frequency: 32kHz – 96kHz
- Five stereo ADC inputs with analogue gain adjust from +24dB to –21dB in 0.5dB steps
- Programmable Limiter or Automatic Level Control (ALC)
- Stereo DAC with independent analogue and digital volume controls
- Stereo Headphone and Line Output
- 3-Wire SPI Compatible or 2-Wire Software Serial Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- Analogue Bypass Path Feature
- Selectable AUX input to the volume controls
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation

APPLICATIONS

- Surround Sound AV Processors and Hi-Fi systems
- DVD-RW

BLOCK DIAGRAM



19-0175; Rev 3; 5/96

MAXIM

±15kV ESD-Protected, +5V RS-232 Transceivers

General Description

The MAX202E–MAX213E, MAX232E/MAX241E line drivers/receivers are designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The various combinations of features are outlined in the *Selection Guide.* The drivers and receivers for all ten devices meet all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbps, when loaded in accordance with the EIA/TIA-232E specification.

The MAX211E/MAX213E/MAX241E are available in 28-pin SO packages, as well as a 28-pin SSOP that uses 60% less board space. The MAX202E/MAX232E come in 16-pin narrow SO, wide SO, and DIP packages. The MAX203E comes in a 20-pin DIP/SO package, and needs no external charge-pump capacitors. The MAX205E comes in a 24-pin wide DIP package, and also eliminates external charge-pump capacitors. The MAX206E/MAX207E/MAX208E come in 24-pin SO, SSOP, and narrow DIP packages. The MAX232E/MAX241E operate with four 1µF capacitors, while the MAX202E/MAX206E/MAX207E/MAX208E/MAX211E/MAX213E operate with four 0.1µF capacitors, further reducing cost and board space.

Applications

Notebook, Subnotebook, and Palmtop Computers
Battery-Powered Equipment
Hand-Held Equipment

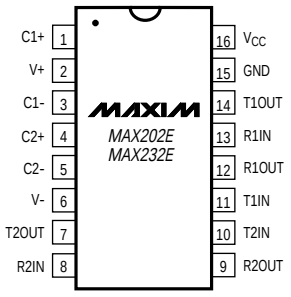
Ordering Information appears at end of data sheet.

Features

- ♦ **ESD Protection for RS-232 I/O Pins:**
  ±15kV—Human Body Model
  ±8kV—IEC1000-4-2, Contact Discharge
  ±15kV—IEC1000-4-2, Air-Gap Discharge
- ♦ **Latchup Free (unlike bipolar equivalents)**
- ♦ **Guaranteed 120kbps Data Rate—LapLink™ Compatible**
- ♦ **Guaranteed 3V/µs Min Slew Rate**
- ♦ **Operate from a Single +5V Power Supply**

Pin Configurations

TOP VIEW



DIP/SO

Pin Configurations and Typical Operating Circuits continued at end of data sheet.

Selection Guide

PART	No. of RS-232 DRIVERS	No. of RS-232 RECEIVERS	RECEIVERS ACTIVE IN SHUTDOWN	No. of EXTERNAL CAPACITORS	LOW-POWER SHUTDOWN	TTL THREE-STATE
MAX202E	2	2	0	4 (0.1µF)	No	No
MAX203E	2	2	0	None	No	No
MAX205E	5	5	0	None	Yes	Yes
MAX206E	4	3	0	4 (0.1µF)	Yes	Yes
MAX207E	5	3	0	4 (0.1µF)	No	No
MAX208E	4	4	0	4 (0.1µF)	No	No
MAX211E	4	5	0	4 (0.1µF)	Yes	Yes
MAX213E	4	5	2	4 (0.1µF)	Yes	Yes
MAX232E	2	2	0	4 (1µF)	No	No
MAX241E	4	5	0	4 (1µF)	Yes	Yes

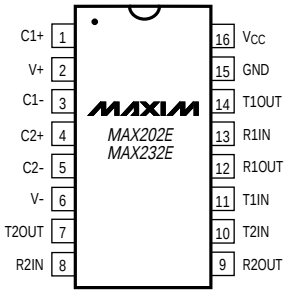
LapLink is a registered trademark of Traveling Software, Inc.

Table 3. DB9 Cable Connections Commonly Used for EIA/TIAE-232E and V.24 Asynchronous Interfaces

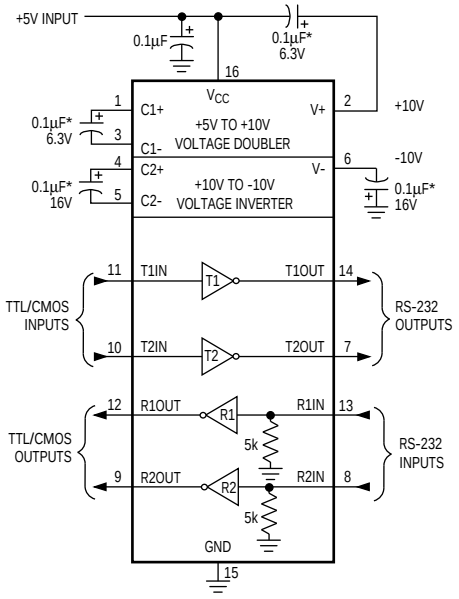
PIN	CONNECTION	
1	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



DIP/SO



PIN NUMBERS ON TYPICAL OPERATING CIRCUIT REFER TO DIP/SO PACKAGE, NOT LCC.
* 1.0µF CAPACITORS, MAX232E ONLY.

TFT LCD Preliminary Specification

MODEL NO.: V270B1 - L01

LCD TV Head Division	
AVP	郭振隆

QRA Dept.	TVHD / PDD		
	DDIII	DDII	DDI
Approval	Approval	Approval	Approval
陳永一	李汪洋	藍文錦	林文聰

LCD TV Marketing and Product Management Division	
Product Manager	陳立宜　　謝芳宜

- CONTENTS -

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 1.0	Jun. 15,'05	All	All	Preliminary Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V270B1- L01 is a TFT Liquid Crystal Display module with 14-CCFL Backlight unit and 1ch-LVDS interface. The display diagonal is 27". This module supports 1366 x 768 WXGA format and can display true 16.7M colors(8-bits colors). The inverter module for backlight is built-in.

1.2 FEATURES

- Excellent brightness (550 nits)
- Ultra high contrast ratio (1000:1)
- Fast response time (8ms)
- High color saturation NTSC 75%
- WXGA (1366 x 768 pixels) resolution
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for both 50/60 Hz frame rate
- Ultra wide viewing angle: 176(H)/176(V) (CR>20) Super MVA technology
- 180 degree rotation display option
- Low color shift function option
- Color reproduction (Nature color)

1.3 APPLICATION

- TFT LCD TVs
- High brightness, multi-media displays
-

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	596.259 (H) x 335.232 (V) (27" diagonal)	mm	(1)
Bezel Opening Area	603.22 (H) x 341.98 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1366 x R.G.B. x 768	pixel	
Pixel Pitch (Sub Pixel)	0.1460 (H) x 0.4365 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	16.7M	color	
Display Operation Mode	Transmissive mode / Normally black	-	
Surface Treatment	Hardness : 3H, Haze : 40% Anti-reflective coating < 2% reflection	-	

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	636.85	637.55	638.25	mm	
	Vertical(V)	379.1	379.8	380.5	mm	
	Depth(D)	33.9	35.4	36.9	mm	To PCB cover
	Depth(D)	39.2	40.7	42.2	mm	To inverter cover
Weight		3700	4000	4300	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

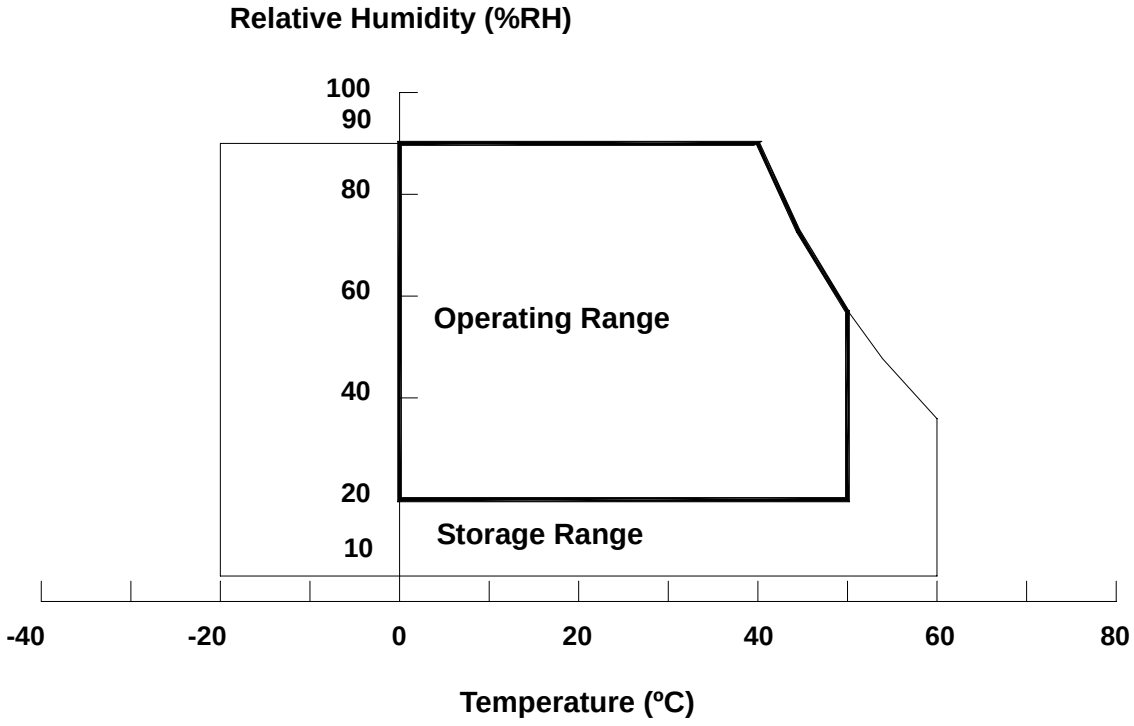
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 60 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 60 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 500 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	6.0	V	(1)
Input Signal Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Lamp Voltage	V_W	Ta = 25 ℃	—	—	3000	V_{RMS}	
Power Supply Voltage	V_{BL}	—	0	—	30	V	(1)
Control Signal Level	—	—	-0.3	—	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals includes Backlight On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

3. ELECTRICAL CHARACTERISTICS

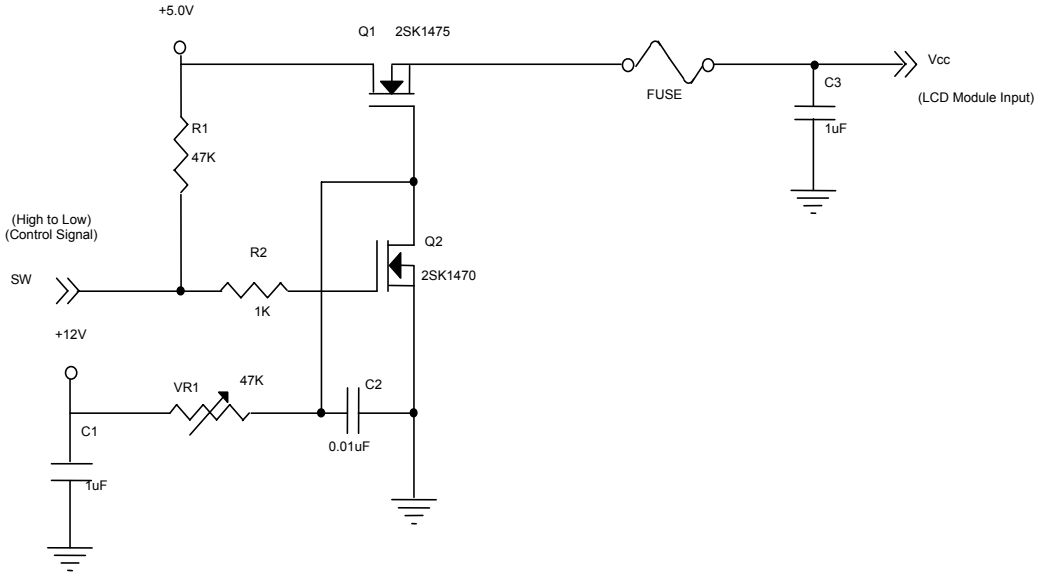
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

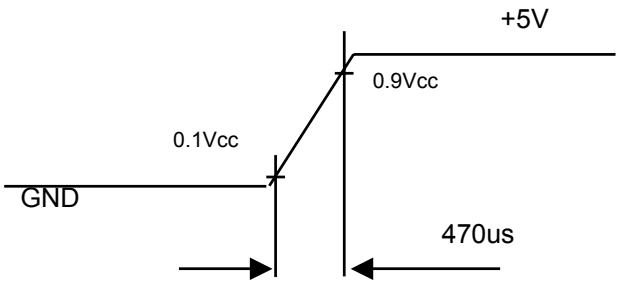
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	4.5	5.0	5.5	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	150	mV	
Rush Current		I_{RUSH}	-	-	3.0	A	(2)
Power Supply Current	White	I_{CC}	-	1.8	-	A	(3)
	Black		-	1.2	-	A	
	Vertical Stripe		-	1.65	-	A	
LVDS Interface	Differential Input High Threshold Voltage	V_{LVTH}	-	-	+100	mV	
	Differential Input Low Threshold Voltage	V_{LVTL}	-100	-	-	mV	
	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T		100		ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 5 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

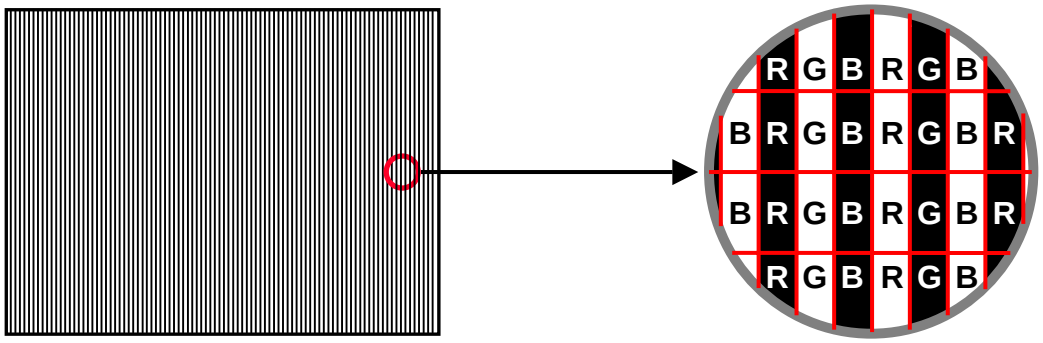
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT INVERTER UNIT

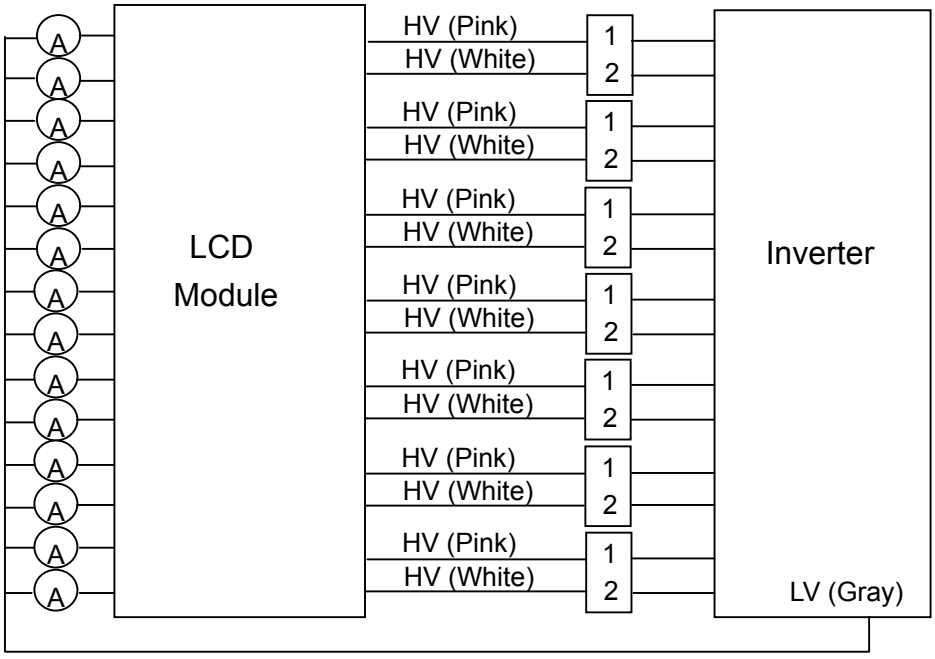
3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	V_W	-	1120	-	V_{RMS}	I_L = 4.7mA
Lamp Current	I_L	4.2	4.7	5.2	mA_{RMS}	(1)
Lamp Starting Voltage	V_S	-	-	1650	V_{RMS}	(2), Ta = 0 ºC
		-	-	1500	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_O	50	-	70	KHz	(3)
Lamp Life Time	L_{BL}	50,000	60,000	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	92	-	W	(5), I_L = 4.7mA
Power Supply Voltage	V_{BL}	22.8	24	25.2	V_{DC}	
Power Supply Current	I_{BL}	-	3.8	-	A	Non Dimming
Input Ripple Noise	-	-	-	500	mV_{P-P}	V_{BL} =22.8V
Backlight Turn on Voltage	V_{BS}	1790	-	-	V_{RMS}	Ta = 0 ºC
		1200	-	-	V_{RMS}	Ta = 25 ºC
Oscillating Frequency	F_W	53	56	59	kHz	
Dimming Frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	10	-	%	

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:



Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second under starting up duration. Otherwise the lamp could not be lighted on completed.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point.) as the time in which it continues to operate under the condition Ta = 25 ±2°C and I_L = 4.2 ~ 5.2 mA_{RMS}.

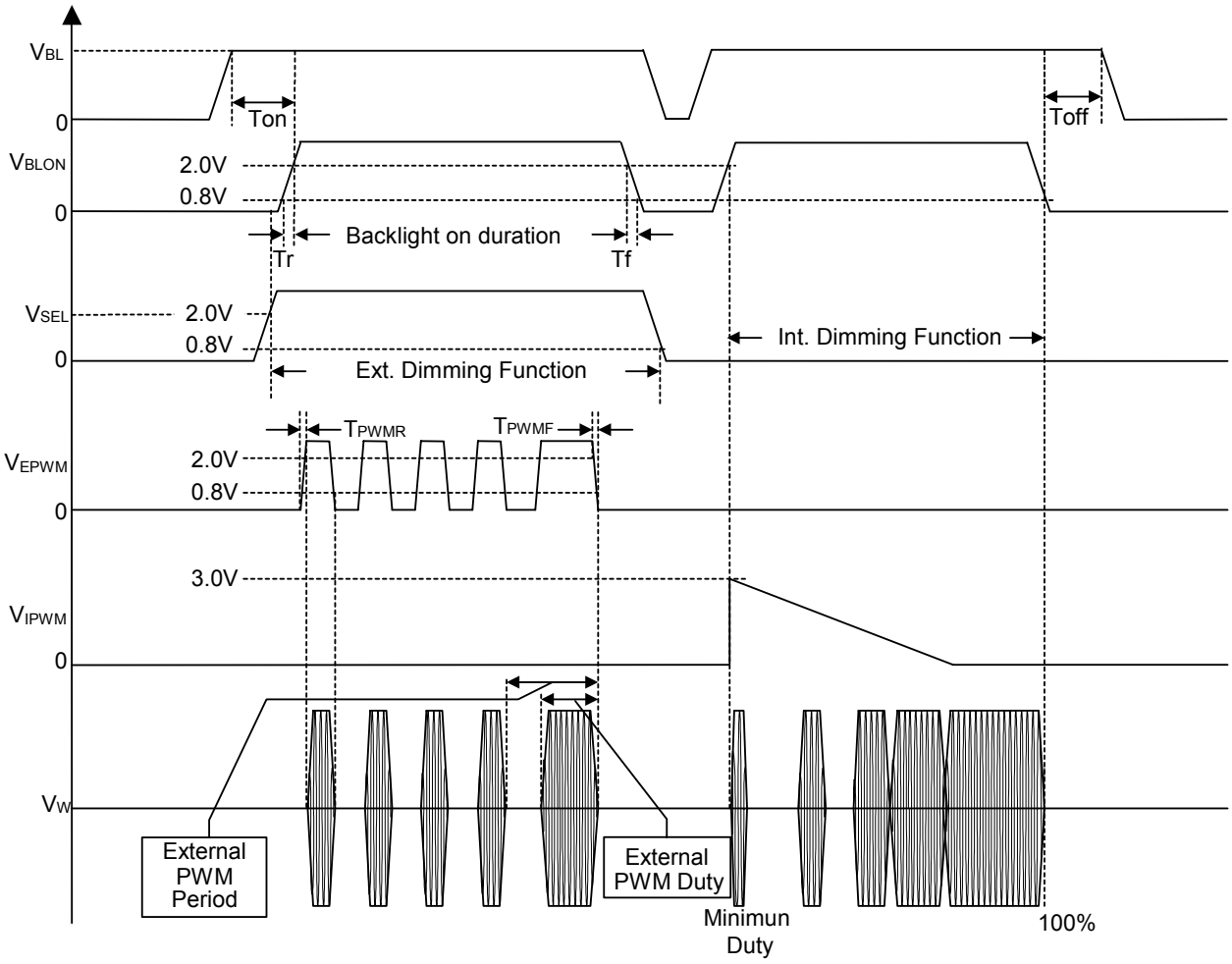
Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

3.2.3 INVERTER INTERTFACE CHARACTERISTICS

Item		Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal/External PWM Select Voltage	HI	V_{SEL}	—	2.0	—	5.0	V	
	LO		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	V_{SEL} = L	—	—	3.0	V	minimum duty ratio
	MIN			—	0	—	V	maximum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	V_{SEL} = H	2.0	—	5.0	V	duty on
	LO			0	—	0.8	V	duty off
Control Signal Rising Time		T_r	—	—	—	100	ms	
Control Signal Falling Time		T_f	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	MΩ	
BLON Delay Time		T_{on}	—	1	—	—	ms	
BLON Off Time		T_{off}	—	1	—	—	ms	

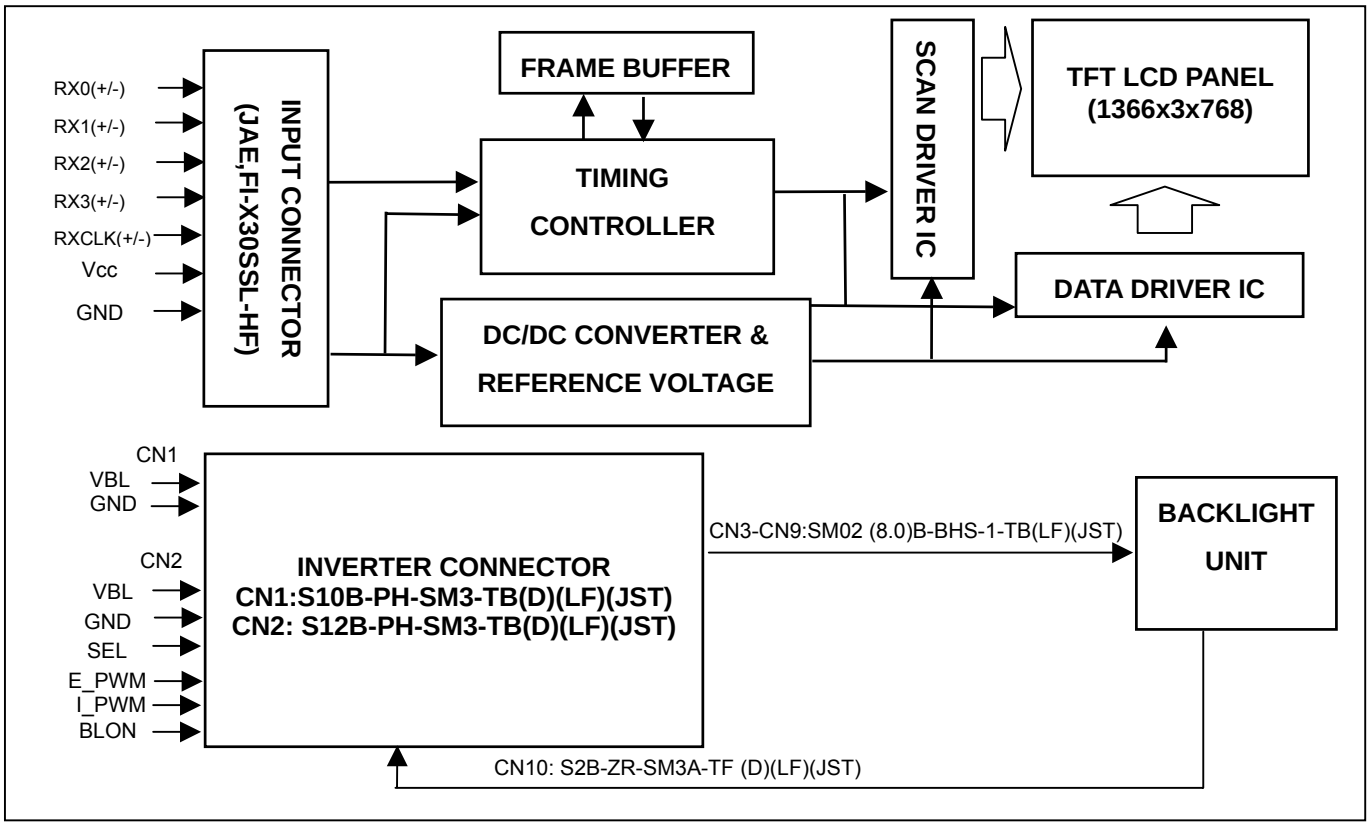
Note (1) The SEL signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM selection (SEL) during backlight turn on period.

Note (2) The power sequence and control signal timing are shown as the following figure.



4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INTERFACE PIN CONNECTION

5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	GND	Ground	
2	RPF	Display Rotation	(3)
3	SELLVDS	Select LVDS data format	(5)
4	NC	No Connection	(2)
5	NC	No Connection	
6	ODSEL	Overdrive Lookup Table Selection	(4)
7	EN_LCS	Low Color Shift	(6)
8	GND	Ground	
9	RX0-	Negative transmission data of pixel 0	
10	RX0+	Positive transmission data of pixel 0	
11	RX1-	Negative transmission data of pixel 1	
12	RX1+	Positive transmission data of pixel 1	
13	RX2-	Negative transmission data of pixel 2	
14	RX2+	Positive transmission data of pixel 2	
15	RXCLK-	Negative of clock	
16	RXCLK+	Positive of clock	
17	RX3-	Negative transmission data of pixel 3	
18	RX3+	Positive transmission data of pixel 3	
19	GND	Ground	
20	GND	Ground	
21	GND	Ground	
22	GND	Ground	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	
26	VCC	Power supply: +5V	
27	VCC	Power supply: +5V	
28	VCC	Power supply: +5V	
29	VCC	Power supply: +5V	
30	VCC	Power supply: +5V	

Note (1) Connector Part No.: FI-X30SSL-HF(JAE) or compatible

Note (2) Reserved for internal use. Left it open.

Note (3) Low : normal display (default), High : display with 180 degree rotation

Note (4) Overdrive lookup table selection. The Overdrive lookup table should be selected in accordance to the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (5) Please refer to 5.5 LVDS INTERFACE (Page 17)

Note (6) Enable Low color shift function.

EN_LCS	Note
L	Low color shift off
H	Low color shift on

5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN3-CN9 (Housing): BHR-03VS-1 (JST)

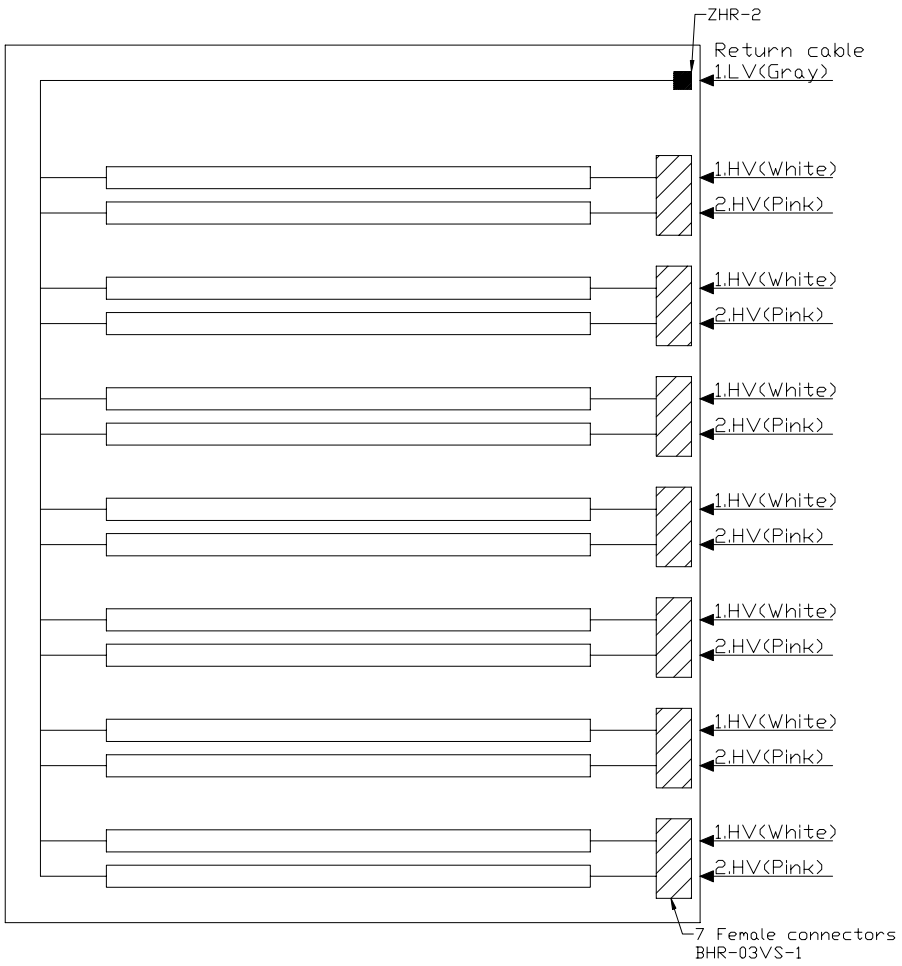
Pin No.	Symbol	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-03VS-1, manufactured by JST. The mating header on inverter part number is SM02(8.0)B-BHS-1-TB(LF) or equivalent.

CN10 (Housing): ZHR-2 (JST) or equivalent

Pin No.	Symbol	Description	Wire Color
1	LV	Low Voltage (+)	Gray
2	NC	No Connection	-

Note (2) The backlight interface housing and return cable for low voltage side is a model ZHR-2 , manufactured by JST or equivalent. The mating header on inverter part number is S2B-ZR-SM3A-TF(D)(LF) or equivalent.



5.3 INVERTER UNIT

CN1(Header):S10B-PH-SM3-TB(D)(LF)(JST) or equivalent.

Pin	Name	Description
1	VBL	+24V Power input
2		
3		
4		
5		
6	GND	Ground
7		
8		
9		
10		

CN2(Header): S12B-PH-SM3-TB(D)(LF)(JST) or equivalent.

Pin	Name	Description
1	VBL	+24V Power input
2		
3		
4		
5		
6	GND	Ground
7		
8		
9	SEL	Internal/external PWM selection High : external dimming Low : internal dimming
10	E_PWM	External PWM control signal E_PWM should be connected to low when internal PWM was selected (SEL = low).
11	I_PWM	Internal PWM control signal I_PWM should be connected to ground when external PWM was selected (SEL = high).
12	BLON	Backlight on/off control

CN3-CN9(Header): SM02(8.0)B-BHS-1-TB(LF)(JST) or equivalent

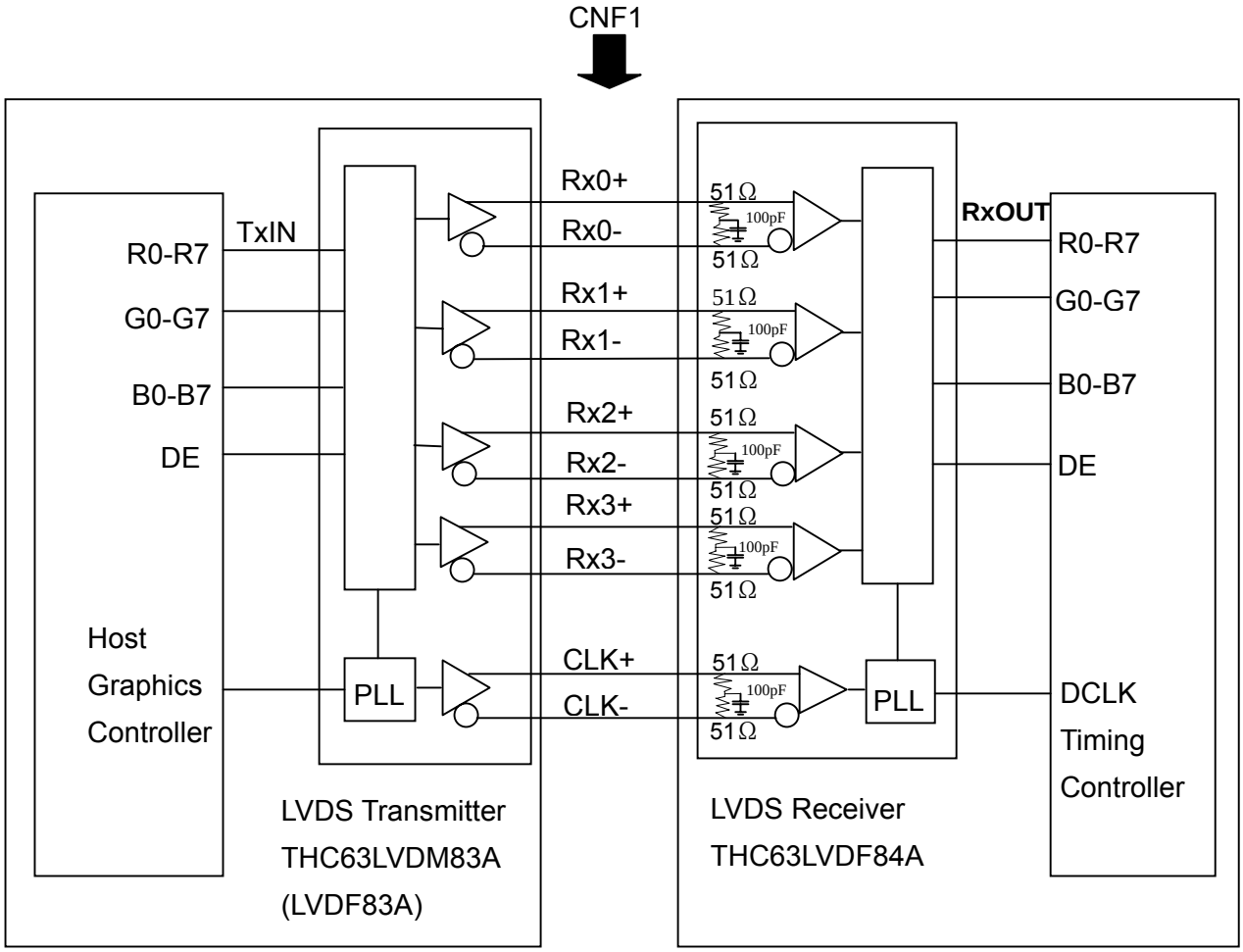
Pin	Name	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

CN10(Header): S2B-ZR-SM3A-TF(D)(LF)(JST) or equivalent

Pin	Name	Description
1	CCFL COLD	CCFL low voltage
2	NC	-

Note (1) Floating of any control signal is not allowed.

5.4 BLOCK DIAGRAM OF INTERFACE



R0~R7 : Pixel R Data ,

G0~G7 : Pixel G Data ,

B0~B7 : Pixel B Data ,

DE : Data enable signal

Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.5 LVDS INTERFACE

	SIGNAL		TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT	
	SELLVDS =L	SELLVDS =H	PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	SELLVDS =L	SELLVDS =H
24 bit	R0	R2	51	TxIN0			27	Rx OUT0	R0	R2
	R1	R3	52	TxIN1			29	Rx OUT1	R1	R3
	R2	R4	54	TxIN2	TA OUT0+	Rx 0+	30	Rx OUT2	R2	R4
	R3	R5	55	TxIN3			32	Rx OUT3	R3	R5
	R4	R6	56	TxIN4			33	Rx OUT4	R4	R6
	R5	R7	3	TxIN6	TA OUT0-	Rx 0-	35	Rx OUT6	R5	R7
	G0	G2	4	TxIN7			37	Rx OUT7	G0	G2
	G1	G3	6	TxIN8			38	Rx OUT8	G1	G3
	G2	G4	7	TxIN9			39	Rx OUT9	G2	G4
	G3	G5	11	TxIN12	TA OUT1+	Rx 1+	43	Rx OUT12	G3	G5
	G4	G6	12	TxIN13			45	Rx OUT13	G4	G6
	G5	G7	14	TxIN14			46	Rx OUT14	G5	G7
	B0	B2	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0	B2
	B1	B3	19	TxIN18			51	Rx OUT18	B1	B3
	B2	B4	20	TxIN19			53	Rx OUT19	B2	B4
	B3	B5	22	TxIN20			54	Rx OUT20	B3	B5
	B4	B6	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4	B6
	B5	B7	24	TxIN22			1	Rx OUT22	B5	B7
	DE	DE	30	TxIN26			6	Rx OUT26	DE	DE
	R6	R0	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6	R0
	R7	R1	2	TxIN5			34	Rx OUT5	R7	R1
	G6	G0	8	TxIN10			41	Rx OUT10	G6	G0
	G7	G1	10	TxIN11			42	Rx OUT11	G7	G1
	B6	B0	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6	B0
	B7	B1	18	TxIN17			50	Rx OUT17	B7	B1
	RSVD 1	RSVD 1	25	TxIN23			2	Rx OUT23	NC	NC
	RSVD 2	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	NC	NC
	RSVD 3	RSVD 3	28	TxIN25			5	Rx OUT25	NC	NC
		DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK	

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE: Data enable signal

Notes(1) RSVD(reserved)pins on the transmitter shall be “H” or “L”.

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

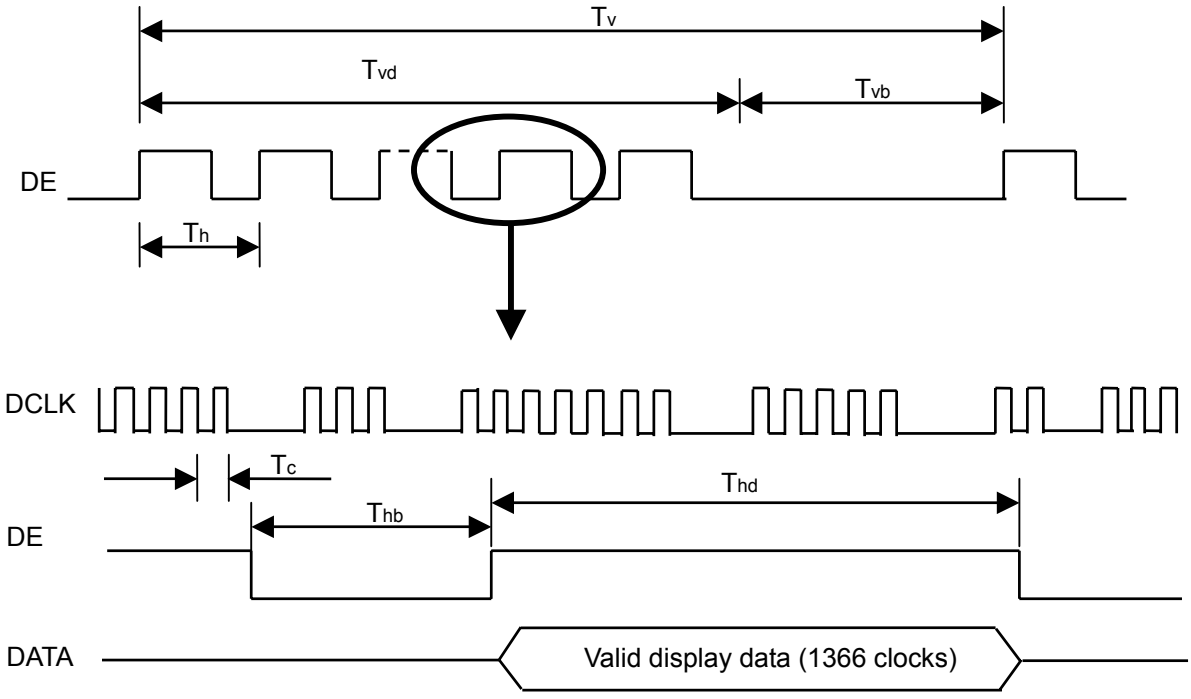
The input signal timing specifications are shown as the following table and timing diagram**.**

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	86	88	MHz	
	Input cycle to cycle jitter	Trcl	-	-	200	ps	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr_5	47	50	53	Hz	(2)
		Fr_6	57	60	63	Hz	
	Total	Tv	770	795	888	Th	Tv=Tvd+Tvb
	Display	Tvd	768	768	768	Th	-
	Blank	Tvb	2	27	120	Th	-
Horizontal Active Display Term	Total	Th	1436	1798	1936	Tc	Th=Thd+Thb
	Display	Thd	1366	1366	1366	Tc	-
	Blank	Thb	70	432	570	Tc	-

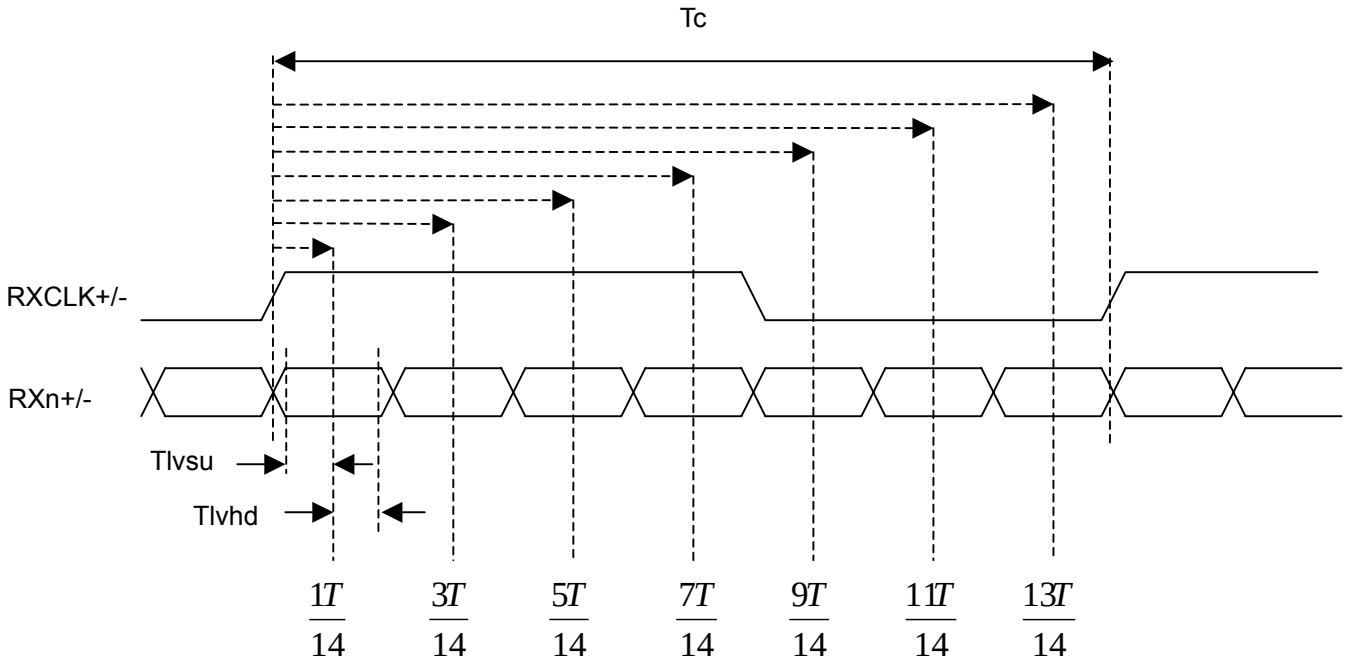
Note (1) Since this module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

(2) Please refer to 5.1 for detail information.

INPUT SIGNAL TIMING DIAGRAM

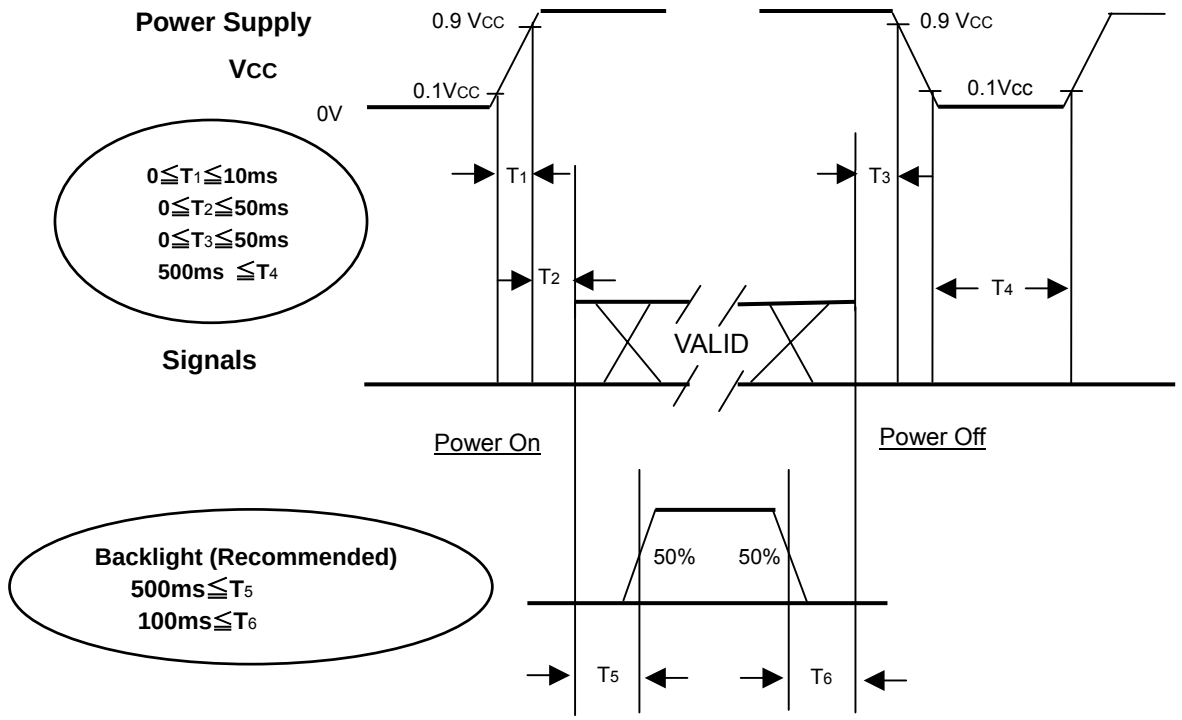


LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	4.7 ± 0.5	mA
Oscillating Frequency (Inverter)	F_W	56 ± 3	KHz

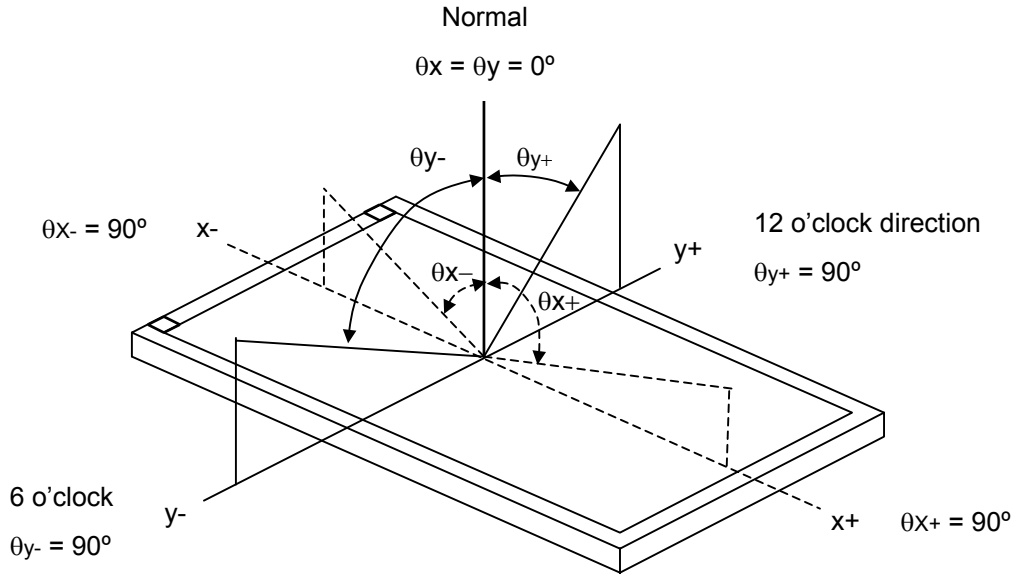
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle		(1000)		-	(2)
Response Time		Gray to gray average			(8)		ms	(3)
Center Luminance of White		L_C			(550)		cd/m^2	(4)
White Variation		δW				(1.3)	-	(7)
Cross Talk		CT				(4)	%	(5)
Color Chromaticity	Red	Rx			(0.652)		-	(6)
		Ry			(0.331)		-	
	Green	Gx			(0.275)		-	
		Gy			(0.597)		-	
	Blue	Bx			(0.143)		-	
		By			(0.063)		-	
	White	Wx			(0.285)		Target	
		Wy			(0.293)			
	Color Gamut	CG			(75)		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20		(88)		Deg.	(1)
		θ_x-			(88)			
	Vertical	θ_Y+			(88)			
		θ_Y-			(88)			

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by EZ-Contrast 160R (Eldim)



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

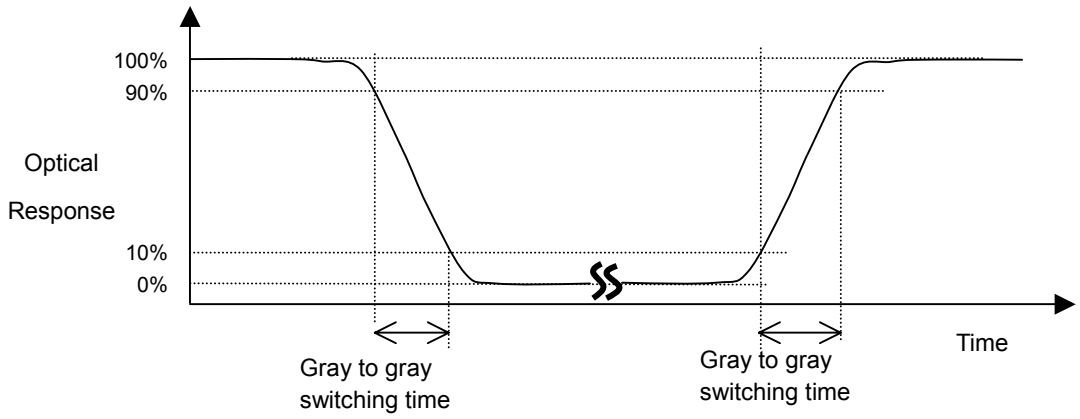
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 63, 127, 191, 255.

Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each other .

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L (5)$

$L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5$

L (x) is corresponding to the luminance of the point X at the figure in Note (7).

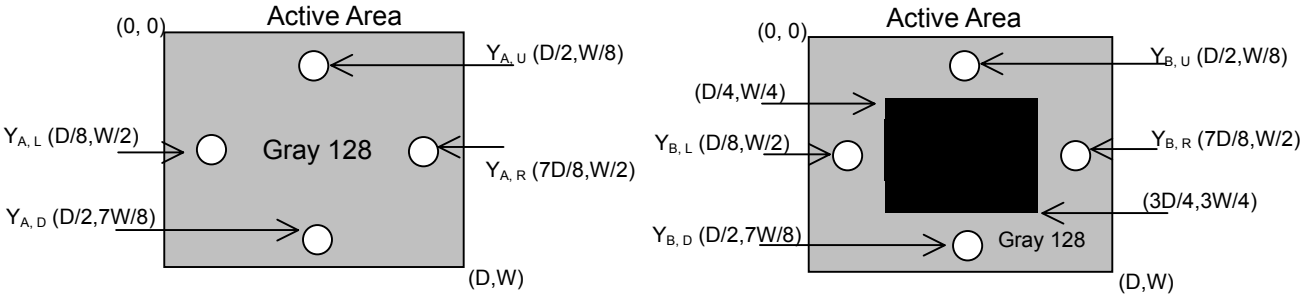
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

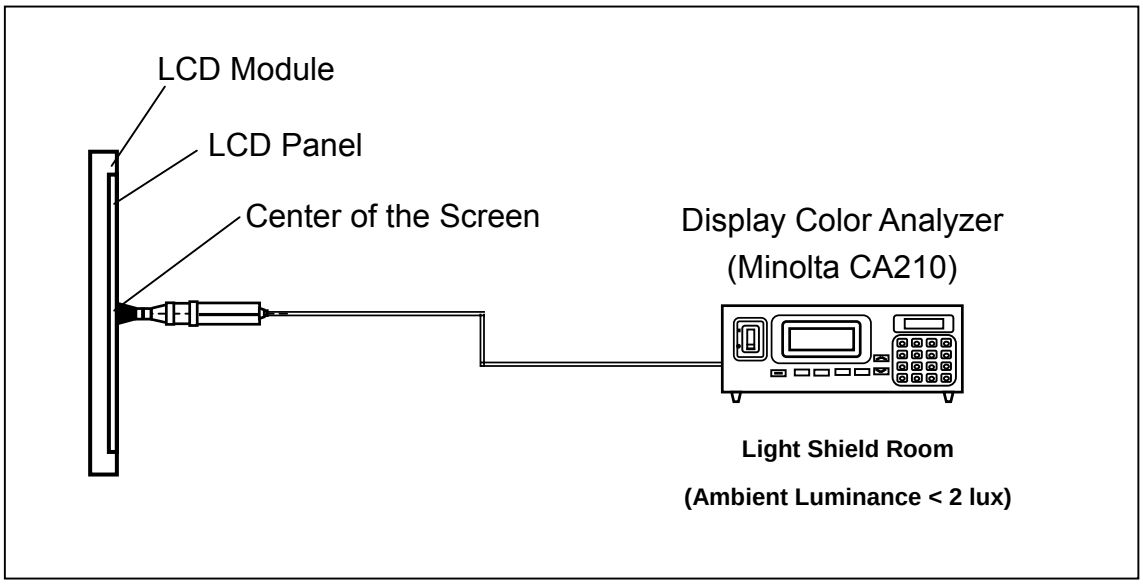
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

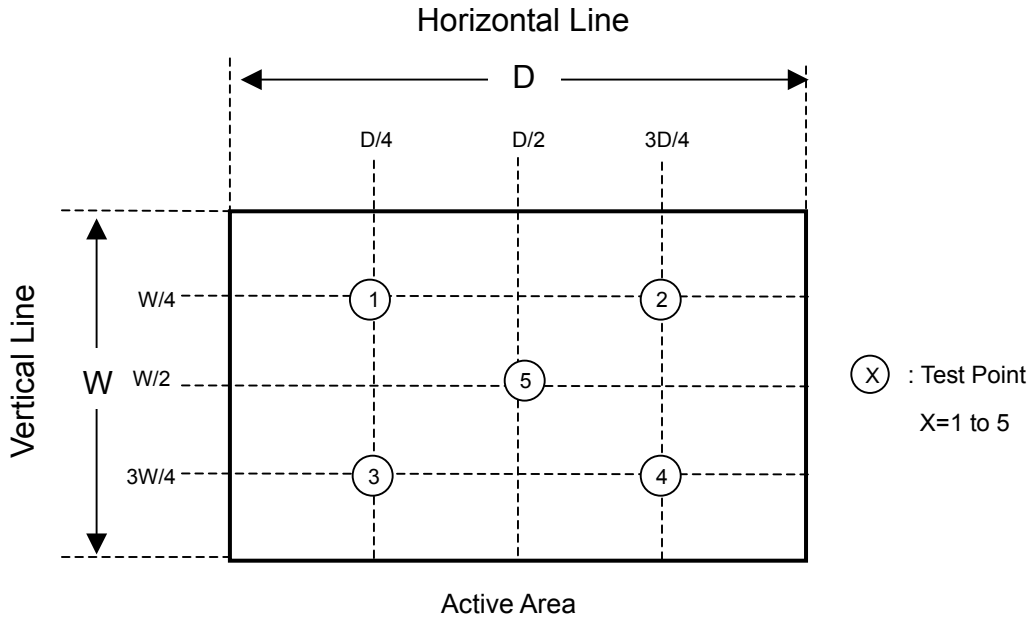
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

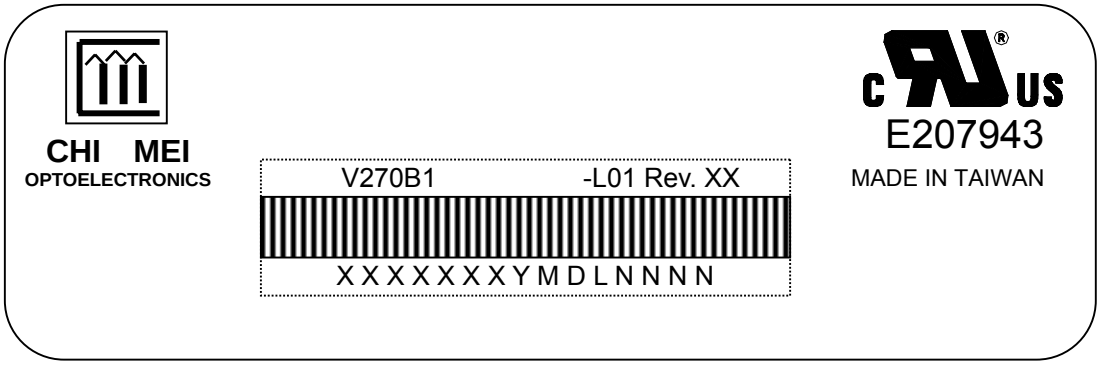
δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

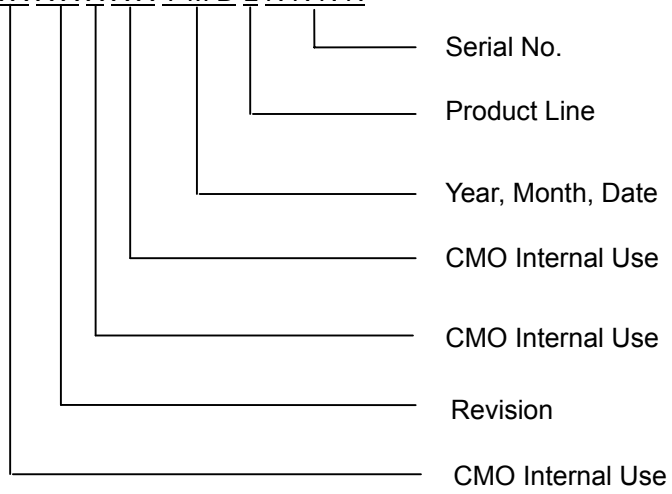
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V270B1-L01

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 4 LCD TV modules / 1 Box

(2) Box dimensions : 742(L) X 327 (W) X 510 (H)

(3) Weight : approximately 19Kg (4 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

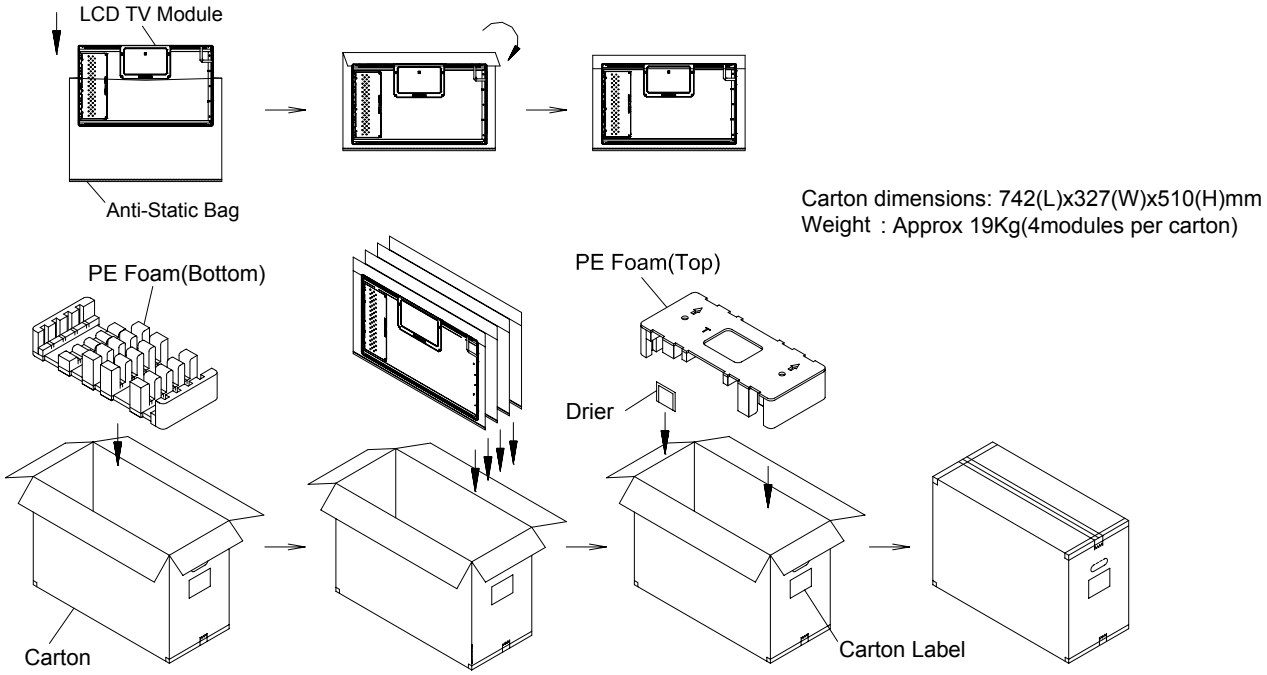


Figure.9-1 packing method

Corner Protector:L1020*50mm*50mm

Pallet:L1100*W1100*H135mm

Corrugated Fiberboard:L1100*W1100mm

Pallet Stack:L1100*W1100*H1160mm

Gross:168kg

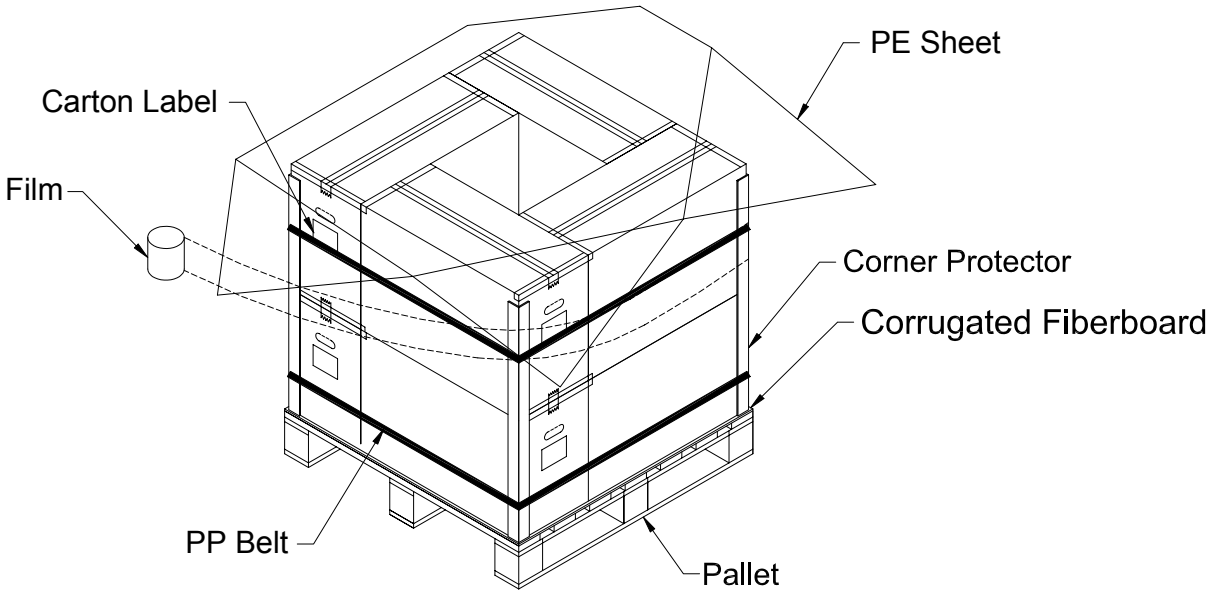


Figure. 9-2 packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

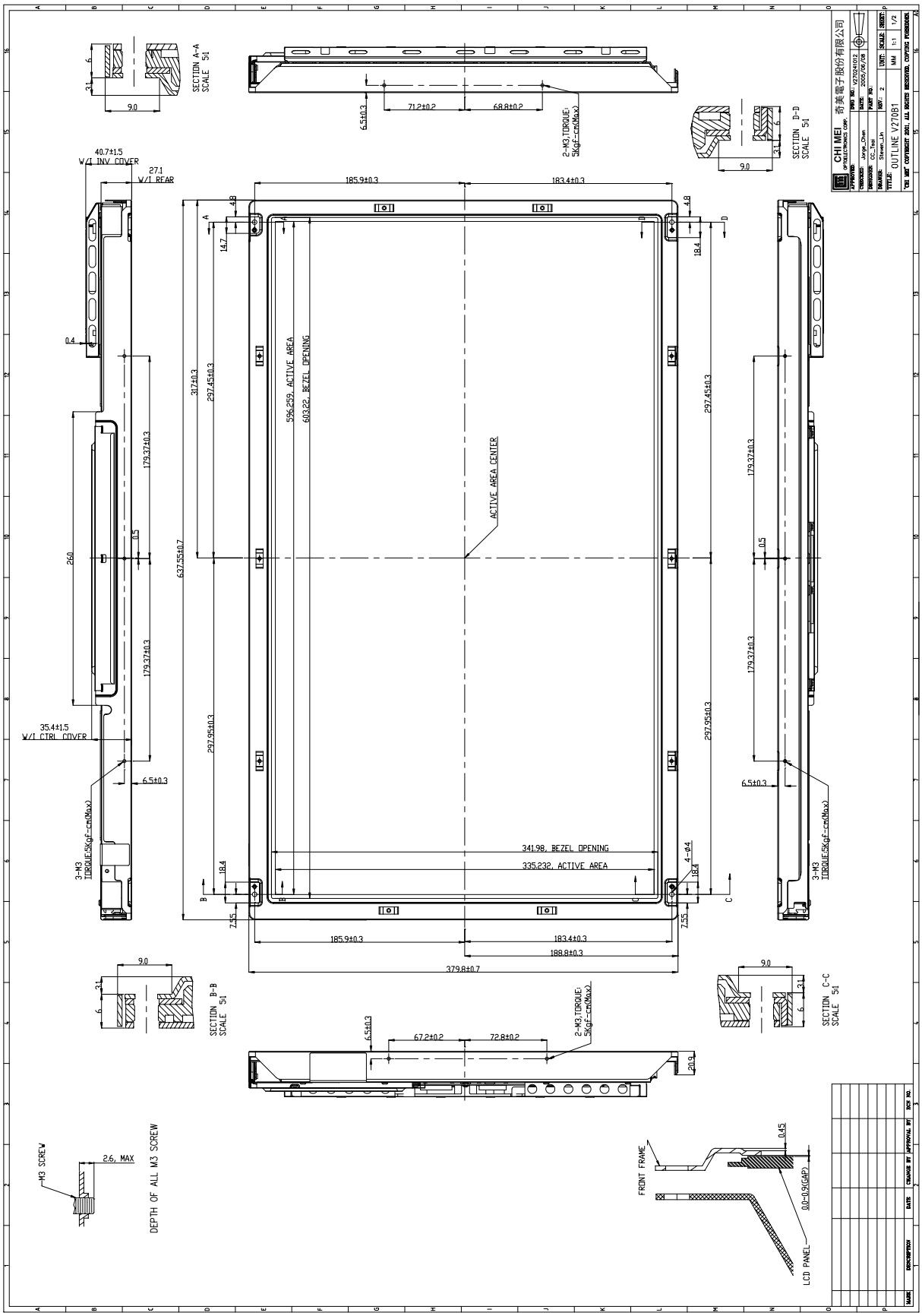
10.2 SAFETY PRECAUTIONS

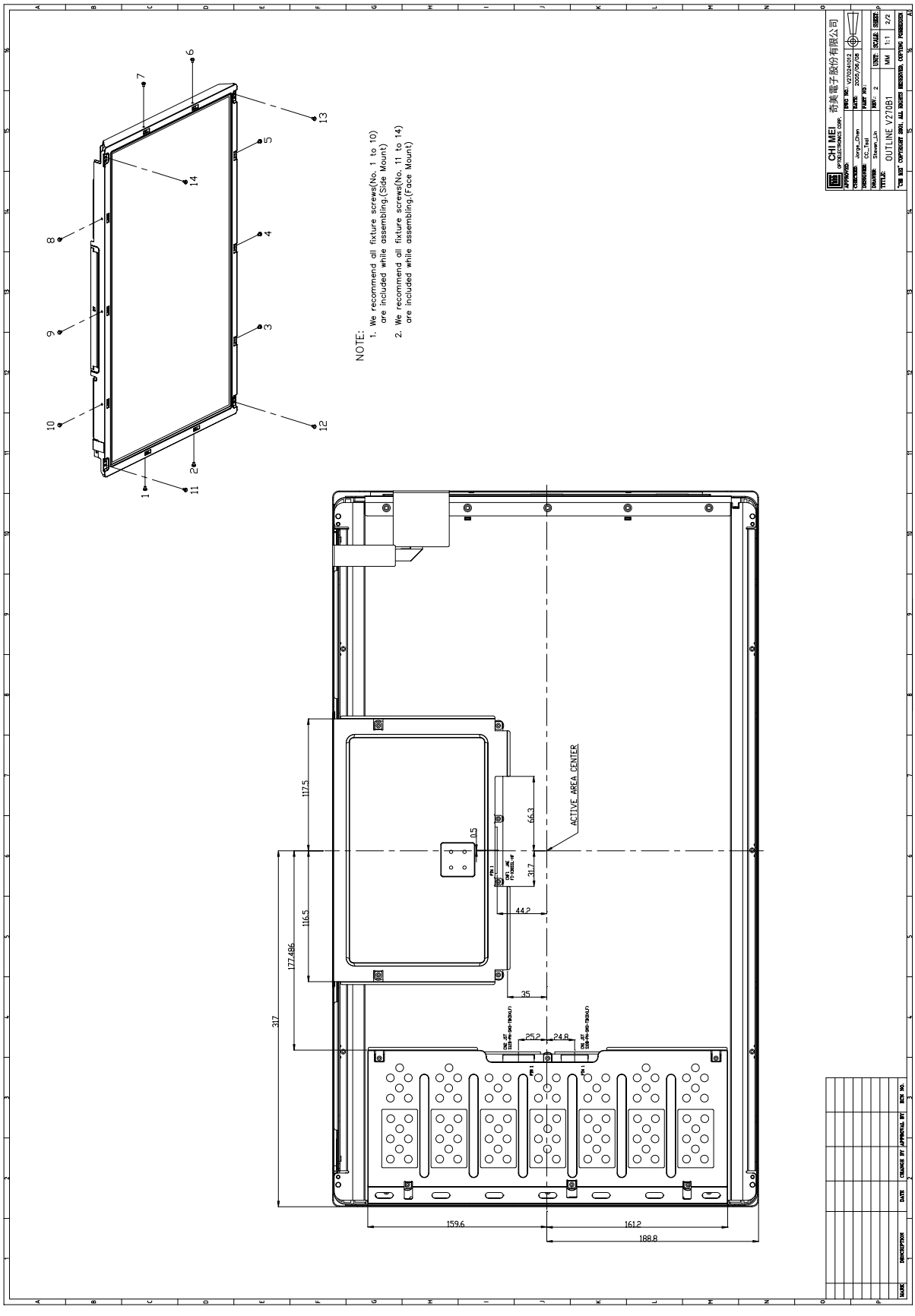
(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

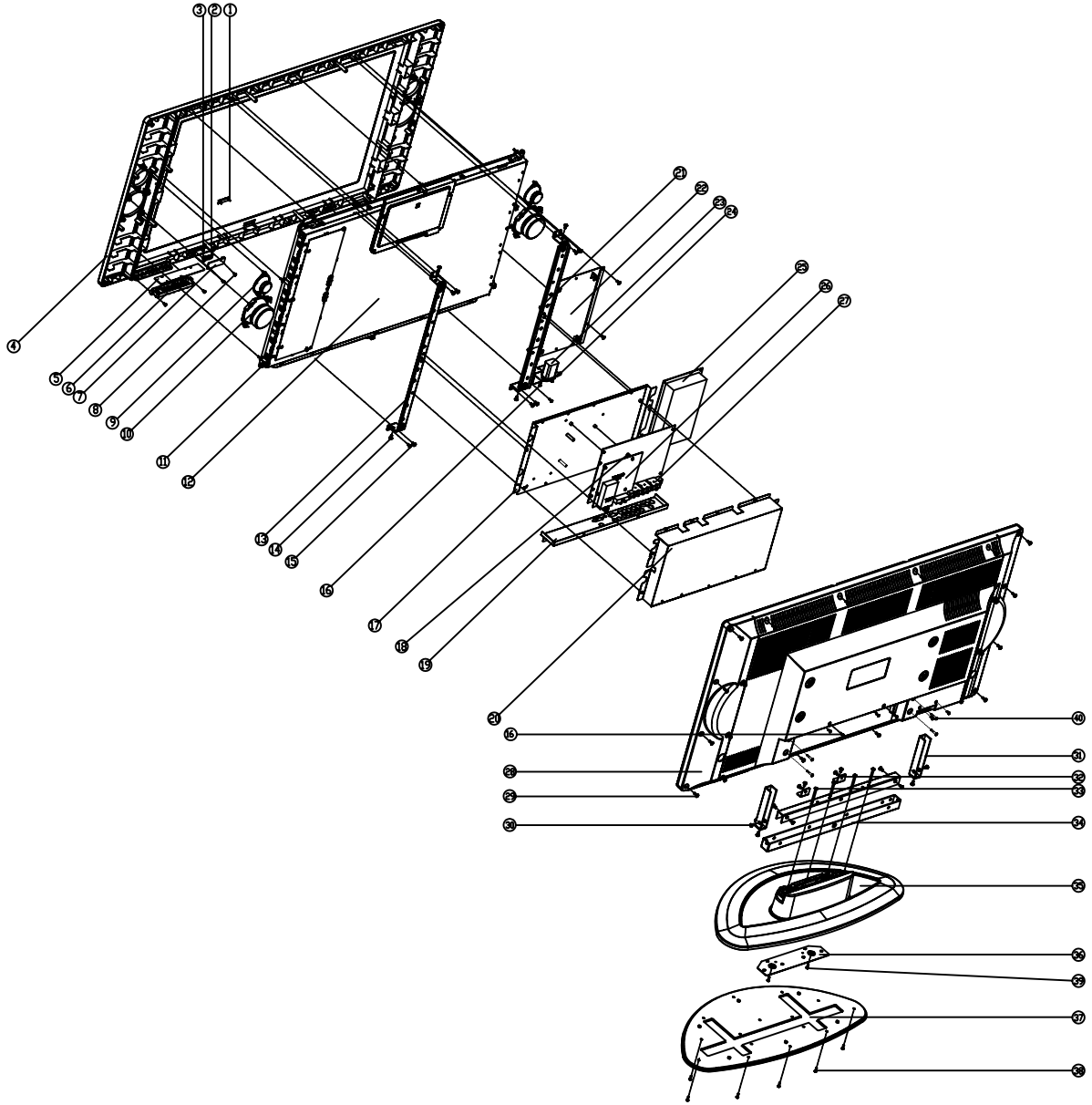
11. MECHANICAL CHARACTERISTICS




NOTE:
1. We recommend all fixture screws(No. 1 to 10) are included while assembling.(Side Mount)
2. We recommend all fixture screws(No. 11 to 14) are included while assembling.(Face Mount)
ACTIVE AREA CENTER
159.6
161.2
188.8
317
177.486
116.5
117.5
66.3
31.7
44.2
35
25.2
24.8
CHI MEI
奇美電子股份有限公司
V270B1-L02
OUTLINE V270B1
2/2

NOTE : THIS RELEASED DRAWING WAS PRODUCED BY COMPUTER,DO NOT UPDATE MASTER MANUALLY.

DWG.Rev.	ZONE	DESCRIPTION	DATE	REVISOR
0		RELEASE	22-Jan-06	



ITEM	PART No.	DESCRIPTION	QTY
40	694-407868-10	MACH SCREW BH 4X8 B ZNP +S	4
39	694-208857-10	SELF TAPPING SCREW BINDING HEAD 3X8ZB BLACK ZN PLATED	14
38	692-329829-10	S-TAP. SCREW BHD 3X8	11
37	429-L38A001-01	BASE SHEET	1
36	429-L38A009-01	SECURE SHEET	1
35	224-L38A001-02RV	STAND BASE COVER	1
34	429-L38A005-01	"U" BUTTON CROSSBEAM	1
33	692-407840-10	MACH SCREW TRS M4X25	4
32	429-L38A003-01	"L" SHEET	2
31	429-L38A002-01	SECURE LEG	2
30	692-407868-10	MACH SCREW M4X8	12
29	694-408412-10	MACH SCREW BID #4X2	20
28	222-L38A00-02AV	BACK CABINET	1
27	E7002-402000	MAIN PCB	1
26	E7002-402001	TUNER PCB	1
25	E7002-402000	POWER PCB	1
24	429-L38A004-01S	POWER/AV JACK BRACKET	1
23	E3029-402003	AC JACK	1
22	426-L38A006-01S	SHIELD BOX BOTTOM (PCMCIA)	1
21	692-302003-10	MACH SCREW PAN M3X5	21
20	493-L38A002-01S	SHIELDING COVER (VSC)	1
19	436-L38A005-01S	TERMINAL SHEET	1
18	649-42500-01	CONNECT BOSS MICO CHASSIS 42IN	1
17	426-L38A002-01S	SHIELDING BOTTOM (VSC)	1
16	692-302008-10	MACH SCREW CTS M3X8	4
15	694-408402-10	S-TAP. SCREW BID 4X8	10
14	694-407838-10	MACH SCREW BID M4X30	4
13	429-L38A001-01S	MAIN BRACKET	2
12	E6250-302306	LCD PANEL	1
11	429-L38A004-01	Z BRACKET	0
10	E4002-324001	LOW SPEAKER	2
9	E4002-654001	HIGH SOUND SPEAKER	2
8	694-208209-10	S-TAP. SCREW BID 2.6X8	4
7	771-L38A00-01	REMOTE CONTROL PCB-ASSEMBLY	1
6	277-42300-01S	FUNCTION KNOB	1
5	E3701-042000	KEY PCB ASSY	1
4	220-L38A004-01AV	FRONT CABINET	1
3	263-42500-01S	POWER LENS	1
2	262-216004-01L	SENSOR LENS	1
1	406-420211-01	NAME PLATE	1

DRAWN										
CHECKED										
APPRD.										

3rd ANGLE PROJECTION

TOLERANCE UNLESS OTHERWISE SPECIFIED	
0 ~ 30	±0.10
30~120	±0.20
120 ~ 400	±0.30
ANGULAR	±0°
UNIT : mm	

KAWA ELECTRONIC R & D CENTRE

MATL.

FINISH

TITLE EXPLODE VIEW

MODEL NO. LCT3205

PART NO. EXP-L38A00-01

SCALE 1/1

DWG NO. L38A00EXP1

SHEET 1 OF 1

Spare Part List for LCT3226

Item	Part Number	Part Description	Usage / unit	Unit
1	E6203-32CD01	DISPLAY LCD 32"	1	piece
2	E7802-005010	MAIN BOARD PCBA	1	set
3	E7802-005011	ATV TUNER BOARD	1	set
4	E7802-005008	POWER PCBA	1	set
5	771-L32AB02-02	KEY PCB ASSY	1	set
6	771-L32AB01-01	REMOTE RECEIVE PCBA	1	set
7	E4101-027001	POWER SWITCH	1	piece
8	E4801-124001	SPEAKER	2	piece
9	E4802-014001	TWEETER	2	piece
10	E3219-002003	POWER SOCKET	1	piece
11	E3461-064016	WIRE FOR TV+COMBO INVERTER	1	piece
12	E3471-000047	WIRE ASSY 30P	1	piece
13	E3421-925038	WIRE ASSY TJC3-2Y L=850MM SPK-L	3	Piece
14	E3461-064018	WIRE FOR TV+COMBO DVD STANDBY POWER WIRE	1	piece
15	E3421-925050	WIRE ASSY 12P	1	piece
16	E3421-925051	WIRE ASSY 4P L=220 (MICO)	1	piece
17	E3421-925052	WIRE ASSY 6P L=240 (MICO)	1	piece
18	E3421-925062	WIRE ASSY L=540 2.0/2.5 4P FOR 32LCD CMO	1	piece
19	E3421-925063	WIRE ASSY L=430/540 2.0/2.5 11P FOR 32LCD CMO	1	piece
20	E3421-925020	WIRE ASSY 300MM 3WIRES FOR POWER CONNECT	1	piece
21	E3421-924009	WIRE ASSY 2P L120	2	piece
22	E3421-229007	WIRE 3P	1	piece
23	E3421-925065	WIRE ASSY TJC3-3Y L=850MM SPK-L	1	piece
24	E3404-157004	AC CORD	1	Piece
25	200-L32AB02-MTD02AV	CABINET FRONT	1	Piece
26	370-42D101-01	RUBBER FOOT	6	piece
27	E7301-010002	BATTERY AAA	2	piece
28	E7501-051001	REMOTE CONTROL	1	set
29	202-L32AB01-01AV	CABINET BACK BLACK	1	piece
30	481-L32AB11-01S	SHIELD BOX BOTTOM(POWER)	1	Piece
31	277-42D101-01S	FUNCTION KEY	1	piece
32	483-L32AB12-01S	SHIELD COVER (VSC)	1	piece
33	481-L32AB02-01S	SHIELDING BOTTOM (VSC)	1	piece

Spare Part List for LCT3226

Item	Part Number	Part Description	Usage / unit	Unit
34	436-L32AB05-01S	TERMINAL SHEET	1	piece
35	423-L32AB01-01S	POWER JACK BRACKET	1	piece
36	269-290804-01L	REMOTE LENS	1	piece
37	263-42D101-01S	POWER LENS	1	piece
38	231-L32AB01-01RV	BASE COVER SILVER	1	piece
39	510-L32AB01-MTU01K	GIFT BOX AKAI	1	piece
40	310-493950-07V	POLYBAG 49"X39"X0.5MM FOR MAIN UNIT	1	piece
41	300-L32AB12-02C	POLFOAM TOP LEFT AND RIGHT	1	piece
42	300-L32AB11-02C	POLFOAM BOTTOM LEFT AND RIGHT	1	piece
43	310-111404-07V	POLYBAG FOR INSTRUCTION MANUAL	1	Piece
44	580-L32ABHM-TU01L	INSTRUCTION MANUAL	1	Piece
45	388-42D103-01H	CAUTION LABLE	1	piece
46	388-L27AB01-01H	POWER PLATE	1	piece
47	387-L32AB01-MTU02H	MODEL PLATE	1	piece
48	384-L32AB01-MTU02H	SHEET FOR CMO PANEL	1	Piece
49	590-L32AB01-01	WARRANTY CARD	1	piece
50	593-L32AB01-02	INSERTION CARD	1	piece
51	579-L32AB02-01	UPC LABEL OF G/B	2	piece
52	568-P46T02-02	WARNING LABEL	1	piece
53	579-42D102-09	SERIAL NO/BAR CODE LABEL	1	piece
54	579-42D105-01	PROTECTIVE EARTH LABE	1	piece

If you forget your V-Chip Password

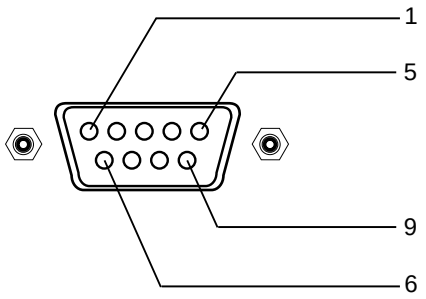
- Omnipotence V-Chip Password: **8205**.
- Press **MENU** button.
- Press **LEFT RIGHT** buttons to highlight "MISC" Menu.
- Press **Up, Down** buttons to highlight "Parentald".
- Press **ENTER** button to pop up "Input your Password Please".
- Use the **Number buttons** (0~9) to enter an omnipotence Password.
- Press **ENTER** button to confirm and your can select "CHANGE PASSWORD".
- Suggest: Change to your familiar Password again.

Software upgrade

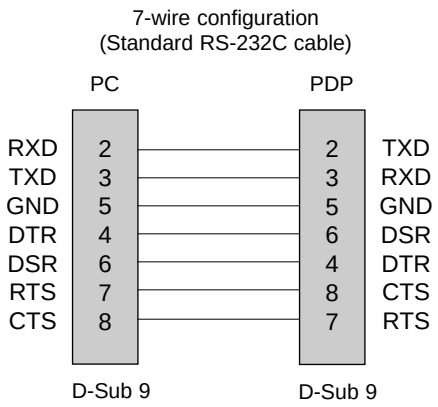
- Connect the RS-232C input jack to an external control device (such as a computer) and software upgrade.

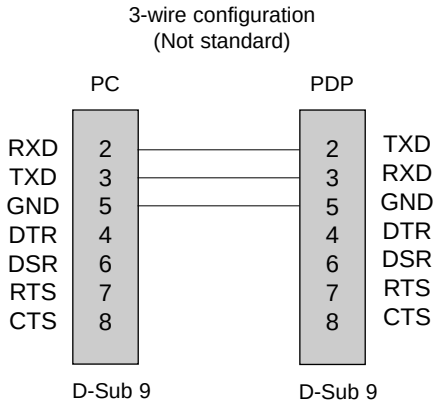
Type of connector; D-Sub 9-pin male

No.	Pin name
1	No connection
2	RXD (Receive data)
3	TXD (Transmit data)
4	DTR (DTE side ready)
5	GND
6	DSR (DCE side ready)
7	RTS (Ready to send)
8	CTS (Clear to send)
9	No Connection



RS-232C configurations





Software upgrade Process

- Power Switch OFF.
- Connect the serial port of the control device to the RS-232 jack on the LCD-TV back panel. RS-232C connection cables are not supplied with the LCD-TV.
- Power Switch ON. The power indicator on the front of the panel should now display red, means that the LCD-TV is in standby mode.
- Copy the software (MTKTOOL) to the computer.
- Open the software (MTKTOOL.EXE)
- Select MTK 8205 and Point "browse" on the interface of the MTKTOOL.exe.
- Select the file which will be update.
- Point "update" on the interface of the MTKTOOL.exe.
- Waiting for the upgrader programing, when it is finished, the bar will display 100%.
- After the upgrader is finished, shut down the power switch, take out the RS-232C connection after the power indicator is extinguished.

Note: After upgrading, the first time of power on will be some long.